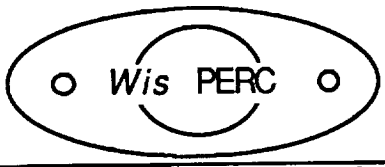

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HIGH POWER DENSITY DC-TO-DC CONVERTERS FOR AEROSPACE APPLICATIONS

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FINAL REPORT

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ABSTRACT

Three new dc-to-dc converter topologies aimed at high-power high-frequency applications are introduced. Major system parasitics, namely, the leakage inductance of the transformer and the device output capacitance are efficiently utilized. All circuits operate at a constant switching frequency, thus simplifying design of the reactive elements. Of the three circuits the single-phase and three-phase versions of the dual active bridge topology demonstrate minimal electrical stresses, better utilization of the transformer, bi-directional and buck-boost modes of operation. The power transfer characteristics and soft-switching regions on the Vout-Iout plane are identified. Wide control range can be achieved for a dc conversion ratio of unity for the dual active bridge topologies.

For the proposed topologies, relatively low magnetizing inductance helps widen the region of lossless control under lightly loaded conditions. However, increased snubber capacitance, for reduced switching losses, diminishes region of lossless control.

Given the converter requirement of high-power densities and low, distributed leakage inductance, coaxially wound transformers are seen to be a potential candidate. Two coaxial transformers with different cross-sections have been built for a rating of 50 kVA. The measured leakage inductance at 50 kHz is seen to be in the vicinity of 150 - 250 nH, with power density of approximately 0.1 kg/kW.

Based on the single-phase dual active bridge topology, a 50kW, 50kHz converter operating at an input voltage of 200Vdc and an output voltage of 1600Vdc was fabricated. The actual power density of 0.243 kg/kW, although meets the target specification of 0.2 - 0.3 kg/kW, is seen to be dominated by device package weight. Accounting for only the silicon weight and device terminal connections (estimated as 25% of total commercial package), an improved gate drivers, the power density can be improved to 0.19 kg/kW. Experimental results indicate that the converter can handle peak power near rated conditions at an overall efficiency in the range of 84-90%. Bi-directional mode of power transfer at low power levels is also demonstrated. Limitations in the performance of the converter is shown to mainly arise from the device package inductance.

The characteristics of current-fed output, make the dual active bridge topologies amenable to paralleling and hence extension to megawatt power levels. Projections to a 1 MW system operating from a 500 Vdc input, at an output voltage of 10 kVdc and a switching frequency of 50 kHz, using MOS-Controlled Thyristors, coaxially wound transformers operating at three times the present current density with forced-liquid cooling, and multi-layer ceramic capacitors, suggest an overall power density of 0.075 - 0.08 kg/kW and an overall efficiency of 96%.

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CHAPTER 1

INTRODUCTION

1.1 Goal

The goal of this work is the development of high power, high frequency dc/dc converters at power levels in the multi-kilowatt to megawatt range for the aerospace industry. The issue of high power density at these power levels has rarely been addressed. The major components in a dc/dc converter, in terms of weight, are the transformer and the filter elements. The key to reducing the weight of these components is, undeniably, in recognizing the need for higher switching frequencies. High frequency operation also allows good system response, good regulator attributes and low acoustic noise levels. However, to maintain an overall high system efficiency and low cooling requirements, the various frequency dependent losses, including semiconductor device switching losses, transformer losses and losses resulting from secondary effects such as diode reverse recovery, need considerable attention.

Device switching losses increase proportionally with frequency. Given the state-of-the-art high speed devices, like Insulated Gate Bipolar Transistors (IGBT) and Metal Oxide Semiconductor Controlled Thyristors (MCT), it is seen that some form of soft-

switching technique, to minimize the switching losses, is mandatory. The underlying principle of soft-switching is to ensure zero-voltage or zero-current conditions on the switching device during its turn-on/turn-off. Such schemes are broadly classified under Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) techniques. Typically, ZVS schemes allow higher frequency operation and lower sensitivity to system parasitics, such as diode reverse recovery effects and device-parasitic-capacitor dump. Soft-switching also results in lower radiated and conducted Electromagnetic Interference (EMI).

The transformer, a necessary element in any high power dc/dc converter for galvanic isolation, is by far the most dominant factor in the power density criteria. The two loss components associated with the transformer are core and copper losses. Since, core losses are a strong function of the frequency and the flux density, various state-of-the-art high frequency core materials, such as Ferrites, Metglas and Permalloy-80 to name a few, need to be investigated. Copper losses, arising from the skin and proximity effects, call for a better understanding of the leakage flux distribution in the winding window. This involves a study of the different winding configurations and conductor types. The losses associated with the secondary effects, mentioned earlier, arise mainly from the interaction of the leakage inductance and diode reverse recovery. The energy trapped in the leakage inductance during reverse recovery of a diode must be

dissipated when the diode snaps off. This results in high voltage stresses in the circuit. Hence, minimization and control over the leakage inductance, in such applications, is also an important issue.

A significant portion of the overall power density is associated with the filter capacitors. The size of these capacitors is governed, mainly by the r.m.s. currents flowing through them. In conventional high power dc/dc converters, commutation-grade capacitors are used which tend to be bulky and lossy. The state-of-the-art multi-layer ceramic (MLC) capacitors offer much higher power densities and need to be investigated for the application of interest.

The prototype converter is rated for an output power of 50 kW at an input voltage of 200 Vdc and output voltage of 2000 Vdc. The overall power density must be in the range of 0.2 - 0.3 kg/kW. The switching frequency has been selected as 50 kHz.

1.2 Organization of Work

A brief survey of the state-of-the-art in the dc/dc converter topologies is presented in Chapter Two. In the light of the given specifications three full-bridge converter topologies, with quasi-square wave (square wave with resonant switching transition) operation, are proposed.

The detailed analysis and operating characteristics of each of the proposed topologies, under ideal conditions, are presented in Chapter Three, with a major emphasis on identifying the soft-switching regions, for each topology on the Output Voltage - Output Current plane. A fundamental model for the dual active bridge topology is also discussed. Finally, a small-signal low-frequency behaviour of the control-to-output and input-to-output transfer functions is presented.

The dependence of the semiconductor device switching and conduction losses on the load and control parameter for the proposed soft-switching topologies are analyzed in Chapter Four.

Chapter Five deals with the issue of selection of the optimum topology from amongst the proposed topologies, based on the requirements of high power density, high efficiency, high reliability and ease of control.

Influence of finite device snubber capacitance and finite transformer magnetizing inductance on the soft-switching regions of operation are addressed in Chapter Six.

Design considerations for high-power high-frequency transformers, with particular emphasis on core material selection, minimization and control of leakage inductance and optimum winding arrangement for minimization of copper losses are addressed in Chapter Seven.

Experimental results from the prototype converter, designed and fabricated for the rated specifications, operating under open loop conditions are presented in Chapter Eight. Limitations on the performance of the converter driven primarily from packaging of the semiconductor device are addressed.

Conclusions and suggestions for future work are summarized in Chapter Nine.

CHAPTER 2

REVIEW OF PREVIOUS WORK

2.1 Introduction

In the light of the design objectives of high power and high power density the existing literature on dc/dc converter technologies is reviewed. Various state-of-the-art hard-switching pwm schemes are examined, and it is seen that the advantage of high power density achievable by increasing the frequency are soon offset by the high switching losses incurred. Recognizing the need for a soft-switching methodology to eliminate the switching losses at the high frequencies of interest, the various resonant and quasi-resonant converters are investigated. The Volt-Amp (VA) stresses experienced by the switching devices and the resonant elements, especially at the high power levels, become intolerably high. The full-bridge converter derived from the resonant pole, which combines the desirable characteristics of hard-switching pwm and soft-switching schemes, is seen to be the most viable option.

2.2 Hard Switching PWM Schemes

Most dc/dc converters in use today are derived from the three basic single quadrant topologies, buck, boost and buck-boost

converters, shown in Fig. 2.2.1 [1]. However, since power transfer is achieved through a single switching device, such circuits are not suitable at the high power levels of interest.

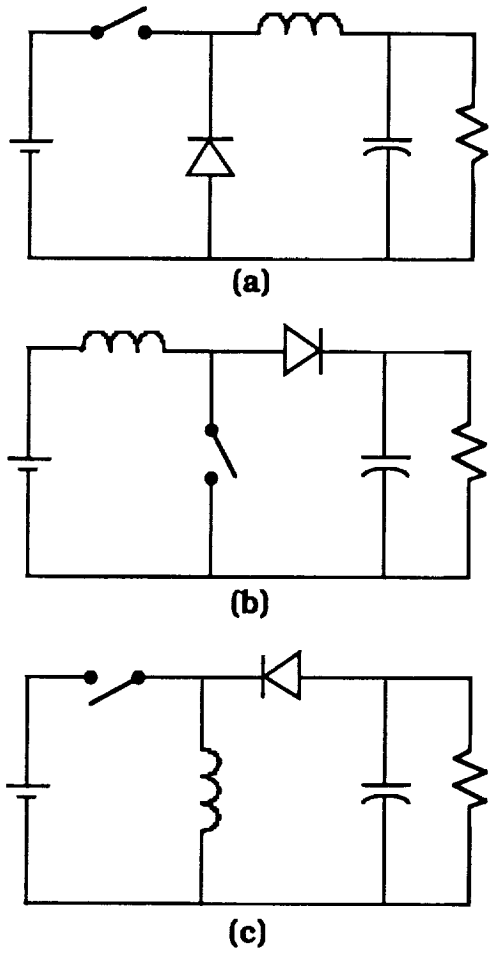


Fig. 2.2.1 Low power hard-switched pwm dc/dc converters : (a) buck (b) boost (c) buck-boost.

At the high power end, the full-bridge (buck-derived) converter with galvanic isolation on the intermediate high frequency a.c. link is

the preferred topology [1] (Fig. 2.2.2). The main advantages of these schemes include constant frequency operation allowing optimum design of magnetic and filter components, minimum VA stresses, good control range and controllability. However, the major drawback of increasing device switching losses with increasing frequency, puts an upper limit on the switching frequency and hence power density. Other problems, which substantially degrade the performance of these converters at high frequencies, are the high voltage stress induced by the parasitic inductances following diode reverse recovery, the additional inductive filter required on the output (besides the capacitor) and the high amounts of electromagnetic interference (EMI) generated from the hard-switching action.

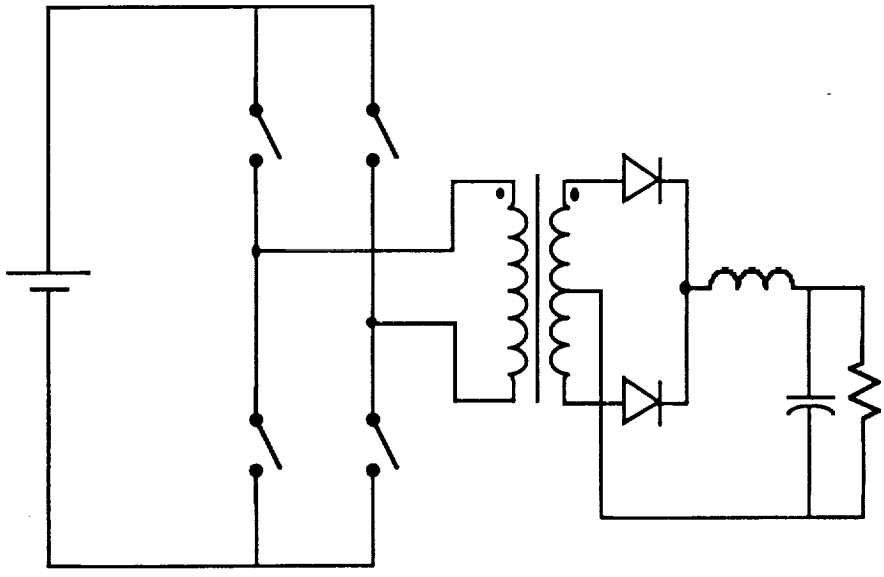


Fig. 2.2.2 Full-bridge (buck-derived) hard-switched pwm dc/dc converter for high power application.

2.3 Soft Switching Schemes

Reactive snubber elements are often used to limit the rate of rise of voltage or current experienced by the switching device in hard-switching pwm strategies. This also provides an easy method of diverting the energy that would be dissipated in the device during the switching transition. However, the energy stored in the reactive snubber elements must typically be dissipated during a subsequent part of the switching cycle. The class of circuits which allow an *automatic and lossless resetting* of the snubber reactive elements through *inherent circuit operation* are referred to as soft switching converters, and are broadly categorized as - Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) converters.

In ZVS schemes the device is made to turn-on and off under near zero-voltage conditions. Fig. 2.3.1a shows a typical implementation. The device is turned-on while its anti-parallel diode is conducting, hence by virtue of the on-state condition of the diode the device sees near zero-voltage. Turn-off is initiated when the device is carrying a certain minimum current. As the device turns off, the remaining load current charges up the purely capacitive snubber, thus limiting the rate of rise of voltage across the device. To ensure near zero-voltage condition, the device must be oversnubbed. Such a scheme inherently requires the load to be inductive, which in fact interacts with the snubber capacitor during turn-off to set up a resonant transition of the voltage. The added benefits of this

switching scheme are prevention of voltage stresses associated with diode reverse recovery effects and elimination of the snubber capacitor charge-dump during turn-on.

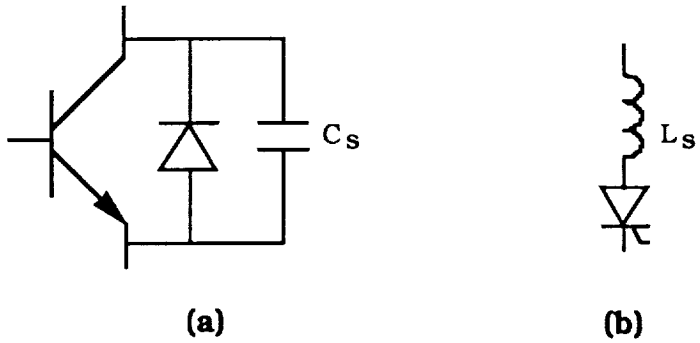


Fig. 2.3.1 Typical soft-switching implementations
(a) Zero voltage switching (ZVS)
(b) Zero current switching (ZCS)

A typical implementation of ZCS scheme is shown in Fig. 2.3.1b. The current through the device is now shaped in a resonant manner, with turn-off occurring naturally at the zero-crossing of the current. At turn-on the series inductance (ideally pure), limits the rate of rise of current through the device. Although, switching losses are virtually eliminated, device reverse recovery effects tend to limit the maximum frequency attainable with ZCS schemes.

Various dc/dc converters, utilizing these schemes, have been reported in the literature in the last decade (selected references are mentioned where appropriate), and will now be investigated as to their suitability for our application.

2.3.1 Resonant DC/DC Converters

The series resonant converter, shown in Fig. 2.3.2, was proposed by Schwarz [2] for high power applications. Since the devices used were thyristors the circuit could only be operated under ZCS conditions, requiring sub-resonance (below resonance) frequency control. Power densities in the 0.9-1.0 kg/kW range at a switching frequency of 10 kHz were reported. Although, these figures can be improved upon by using state-of-the-art high speed devices, high frequency magnetic material and filter capacitors (like multi-layer ceramics), the high VA stresses experienced by the LC-resonant elements and the high current stresses on the devices are a major drawback, especially at the high power levels of interest. For instance, for a 50 kW dc/dc series resonant converter, the kVA rating of the resonant capacitor is approximately 125 kVA, while that for the inductor is 80 kVA. The peak device VA stress is 110 kVA. The component over-rating is seen to constitute a substantial penalty. Moreover, since control of power transfer is achieved by variation of frequency, design of the magnetic and filter elements and EMI-suppression over a wide frequency range become difficult issues.

The parallel output series resonant converter reported by Ranganathan, et al [3], and later extended by Steigerwald [4] to operate under ZVS conditions with gate turn-off devices (Fig. 2.3.3), also suffer from the same problems as the series output series

resonant converter. In particular, at lightly-loaded conditions the energy circulating in the resonant components is substantial requiring wide frequency variations. Current-fed topologies have been discussed by Kassakian [5] and Divan [6].

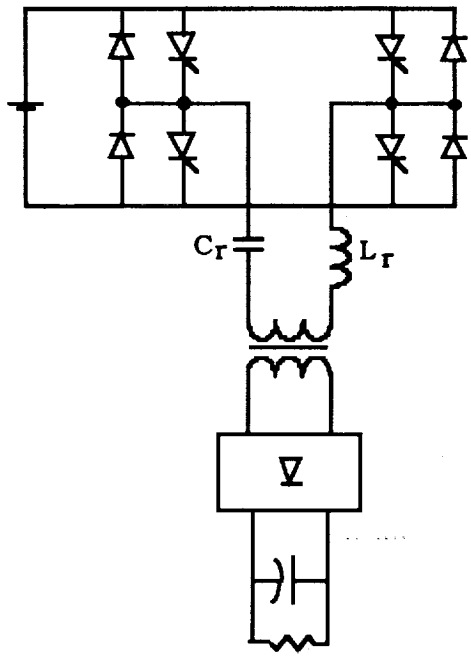


Fig. 2.3.2 Full bridge series output series resonant dc/dc converter

As seen, in all of the above circuits the underlying philosophy of power transfer through a resonant circuit, requires that the devices and the resonant elements be rated for a substantially higher VA rating compared to the delivered power. The higher ratings and the higher device conduction losses impose not only an upper limit on

the achievable power density but also cost penalties reducing the economic potential of these topologies.

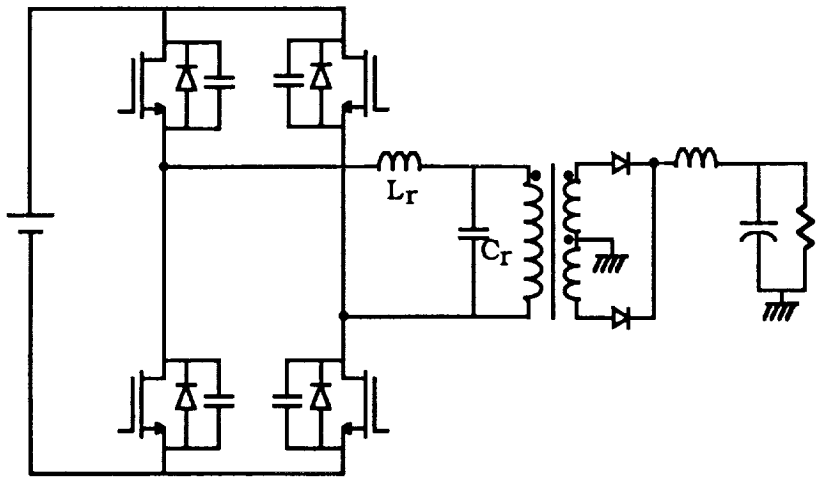


Fig. 2.3.3 Full bridge parallel output series resonant dc/dc converter using gate turn off devices.

2.3.2 Quasi-Resonant DC/DC Converters (QRCs)

Recognizing the advantage of minimal component ratings with conventional hard-switched pwm techniques on the one hand, and the reduced switching losses with resonant converters on the other, the need for a topology with both characteristics was realized. A step in this direction was initiated by Liu and Lee, when they first reported the ZCS - QRCs [7,8] followed by its dual ZVS-QRCs [9]. Fig. 2.3.4 shows an example of each of these converters derived from the basic buck circuit. These circuits are typically aimed at low power

applications and utilize the frequency as a control variable. The ZCS-QRC schemes are susceptible to problems related with diode reverse recovery, capacitive turn-on losses and parasitic oscillations caused by the device output capacitance, and are hence limited in the maximum conversion frequency.

On the other hand, the ZVS schemes shape the device voltage for zero-voltage turn-on at the expense of excessive voltage stresses if designed over wide load variations. The voltage stress can be 11 times the input voltage for a 10:1 load variation. Moreover, the regulation and stability are adversely affected by parasitic oscillations between the resonant inductor and the rectifying diode junction capacitance. For higher output power the half-bridge version of ZCS-QRC presented in [10], requires wide frequency range for wide input voltage and load variations penalizing design of filters and control loops with high gains and wide bandwidths. In [11], the half-bridge ZVS-QRC is shown to maintain zero-voltage switching over a very limited load range, which is further restricted by undesirable parasitic oscillations.

2.3.3 Multi-Resonant DC/DC Converters (MRCs)

Tabisz and Lee introduced the ZVS-Multi-Resonant technique [12], Fig. 2.3.5, to overcome the limitations of the QRCs. In essence, this technique allows zero-voltage switching conditions

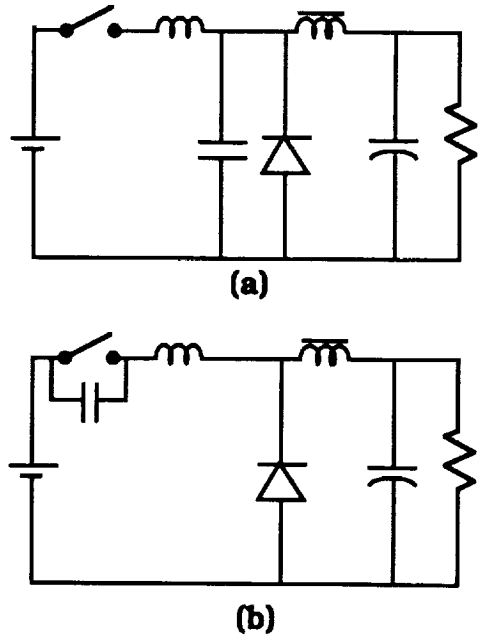


Fig. 2.3.4 (a) Buck-derived Zero-current switching Quasi-resonant dc/dc converter. (b) Buck-derived Zero-voltage switching Quasi-resonant dc/dc converter.

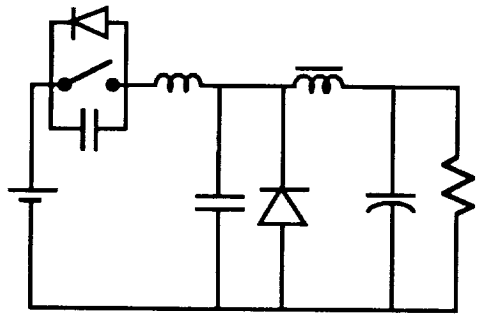


Fig. 2.3.5 Buck-derived Zero-voltage switching Multi-resonant dc/dc converter.

simultaneously for both the active device and the rectifying diode, by utilizing all the dominant parasitics, like, transformer leakage inductance, device output and diode junction capacitances. However, even though operation over a wide load range is possible with limited frequency variation, the switch voltage stresses can be as high as 3-5 times the input voltage.

2.3.4 Quasi-Square Wave Converters

To limit the switch voltage stresses in the single-ended ZVS-MRCs, push-pull and bridge-type configurations were studied by Jovanovic, et al [11,13]. The voltage across the non-conducting switch is automatically clamped to the input voltage by conduction of its complementary switch. In effect, this leads to quasi-square wave (square-waves with resonant transitions) operation. Substantial frequency modulation is still required to operate over a wide load range, thus hampering effective design of EMI-filters and magnetic components.

Recently, Patterson, et. al. [14] introduced the pseudo-resonant dc/dc converter (see Fig. 2.3.6) which demonstrates the possibility of realizing conventional pwm control with resonant switching transitions. The circuit utilizes the concept of the resonant pole [15], and is seen to be amenable for high power applications. Moreover, as mentioned earlier, very high frequency operation is easily attainable given the ZVS characteristics of the topology. With the device turn-

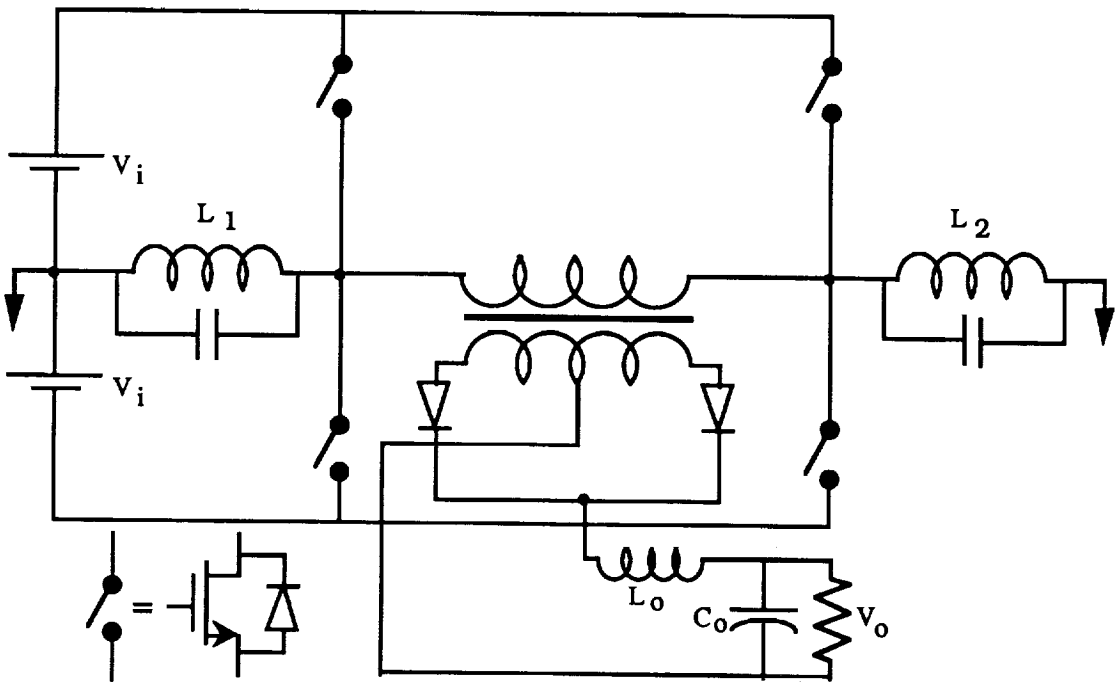


Fig. 2.3.6 Pseudo-resonant dc/dc converter.

on synchronized with its anti-parallel diode conducting, reverse recovery effects associated with the diode are virtually subdued. More importantly since the converter operates under a pwm control strategy, a wide range of operation is achievable unlike the resonant converters where frequency is the control parameter. This also simplifies the task of designing the magnetic and filter elements.

2.4 Component Technology

The power density achievable in high frequency dc/dc converters is typically limited by the state of component technology. In particular the devices, magnetic materials and capacitor technology dramatically influence the frequency, and thus the size of the converter. At higher power levels, these limitations are particularly severe. The device has been one of the major limitations in the past. The only reliable and rugged device in the past has been the thyristor. This has prompted its use in the series resonant converter, with good success. With the introduction of newer gate turn-off devices such as Bipolar Junction Transistors (BJT's) and Insulated Gate Bipolar Transistors (IGBT's), the performance achievable has been significantly advanced. Under soft switching conditions, the BJT has been used at frequencies approaching 30 kHz in multi-kilowatt applications [16]. For the IGBT based converters, it seems possible that frequencies as high as 50 kHz may

be feasible at power levels of up to 50 kW. The possible advent of newer devices such as the (MCT) may enhance the possibilities even more.

One of the major limitations in high frequency designs has been the lack of good magnetic core materials. Ferrites have been very popular for low power applications, and are good at frequencies ranging from the tens of kilohertz to a few megahertz. However, the low flux densities and fragility of the core have limited its use in high power applications. At frequencies in the 10-20 kHz range, other core materials such as Permalloy-80/20 have shown a lot of promise in high power applications. Newer amorphous materials such as Metglas also raise the possibility of raising the frequency to the 50 kHz range. Another aspect of magnetic design which can contribute significantly to the power density is the fabrication technique. The use of co-axial winding techniques hold great promise for high power high frequency transformers.

The choice of capacitors for resonant and filter applications has been rather restricted in the past, especially for high power applications. Only the commutation grade capacitors could realize the high current ratings of interest. The size and weight associated with these capacitors was one of the major limitations in the quest for high power densities. The availability in recent years, of multi-layer ceramic (MLC) capacitors has seen gains in power densities of more than an order of magnitude. For applications where power

density is the paramount concern, MLC capacitors offer a very attractive alternative.

Given advances in component technology, it is important to select the converter topology so that the components are well utilized. The use of topologies that over stress components is bound to result in poorer power densities than topologies where the components are well utilized. The major thrust of this research effort is in the quest for dc/dc converter topologies which feature good component utilization and which offer the benefits of soft switching at the same time.

2.5 Proposed DC/DC Converter Topologies

Recognizing the potential of the resonant pole, three new dc/dc converter topologies suitable for high power applications are proposed [17, 18]. These topologies meet basic requirements for high power dc/dc converters which could potentially realize high power densities. These features include the use of a full bridge for minimum device stresses, constant frequency operation for efficient design of transformers, filter components and system controllers, the use of all major system parasitics and the use of a minimal converter topology. The concept of a minimal converter topology is important for higher power densities, because it uses only those

components which are absolutely essential for a dc/dc conversion function. The three proposed topologies, which satisfy these basic criteria, are introduced below.

2.5.1 Proposed Topology A - Single-Phase Single Active Bridge DC/DC Converter

In the pseudo-resonant dc/dc converter [14], since the transformer is coupled to the output filter inductor (which essentially behaves as a current source), large voltage spikes are induced by the leakage inductance of the transformer at every switching of the output diode bridge. This problem worsens in the presence of diode reverse recovery effects. Hence, the leakage inductance needs to be minimized, requiring good transformer design techniques. Additional inductors L_1 and L_2 (shown in Fig. 2.3.5) are also required to achieve soft-switching of the input bridge devices over a reasonable control range. Overall, the circuit tends to be quite complex and does not lend itself easily to high power applications.

Transferring the output filter inductor to the ac side (in effect lumping it with the leakage inductance), completely changes the operating characteristics of the converter. Energy stored in this equivalent leakage inductance can be naturally and in a lossless manner transferred to the load. Also, reasonable control range can be

realized under soft-switching conditions with this sole effective leakage inductance. The above modification of the pseudo-resonant dc/dc converter suggests its suitability for high power applications, and is our new proposed Topology A, shown in Fig. 3.2.1a. Power flow is governed by the phase-shift between the two resonant poles of the input bridge.

2.5.2 Proposed Topology B - Single-Phase Dual Active Bridge DC/DC Converter

The concept of active control on both the inversion and rectification ends of high power dc/dc converters was first introduced by Peterson, et. al. [19]. Moreover, observing that the circuit of Topology A naturally handles the diode recovery process, it is proposed that if the diodes are replaced by active devices [20] then a much simpler control strategy can be devised. The input and active output bridges can generate fixed-frequency quasi-square waves (with resonant switching transitions) which are phase-shifted from each other. The power transfer can now be controlled by controlling this phase-shift. Also, given the symmetrical nature of the converter, bi-directional power flow can be achieved. Fig. 3.3.1a shows a circuit schematic of this new proposed topology.

2.5.3 Proposed Topology C - Three-Phase Dual Active Bridge DC/DC Converter

This topology is a three phase extension of Topology B (see Fig. 3.4.1a). At the time this circuit was introduced, it was felt that it had the potential of realizing the highest power density considering the much lower filter capacitor requirements, and the state-of-the-art in high power density capacitors then being considered as the commutation grade type. However, with the recently available Multi-Layer Ceramic (MLC) capacitors, it is seen that Topology B can achieve comparable power densities with the added advantage of a simpler transformer. Nevertheless, for the sake of completeness this topology will also be fully analyzed and compared with the other two proposed topologies.

It must be mentioned here that the dual of topologies A and B using thyristors have been analyzed and implemented for superconducting magnetic energy storage (SMES) systems [21,22,23].

To conclude this section, all the three proposed topologies possess the following desirable features:

- virtually zero switching losses for all devices
- use of transformer leakage inductance as the main energy transfer element, potentially capable of higher power densities
- operate at constant frequency in a pwm manner

- high efficiency (no trapped energy)
- low sensitivity to system parasitics
- possibility of paralleling, as a result of the current transfer mechanism

In addition, the dual bridge topologies exhibit

- two-quadrant operation
- buck-boost operation
- smaller transformer and filter.

The focus of this work is the selection and implementation of a suitable converter topology to meet the desired objectives. With this in mind, the three proposed topologies are analyzed in detail to provide a theoretical basis for comparison and selection.

CHAPTER 3

STEADY STATE ANALYSIS OF PROPOSED TOPOLOGIES

3.1 Introduction

This chapter presents the analysis of the steady state operating characteristics of the three proposed dc/dc converter topologies [17] :

(a) Single-Phase Single Active Bridge DC/DC Converter (Topology A)

(b) Single-Phase Dual Active Bridge DC/DC Converter (Topology B)

(c) Three-Phase Dual Active Bridge DC/DC Converter (Topology C)

These topologies are "minimal" in structure in that they consist of the input and output filter capacitors, the two device bridges (active and/or passive, and single or three phase versions) and a transformer, all components essential for a dc/dc converter. They all operate at a constant switching frequency and exhibit soft switching for reduced switching losses. The circuits utilize the leakage inductance of the transformer as the main energy transfer element thus rendering the filters on both the input and output sides purely capacitive.

Since high power density is a crucial requirement, it is important to minimize the device switching losses by adopting a soft-switching methodology. In the proposed topologies all semiconductor devices can operate under conditions of zero-voltage switching. To elaborate, the turn-on of any active device such as MOSFET, BJT, IGBT, MCT is initiated while its anti-parallel diode is conducting. This ensures that the active device naturally takes over as the diode current reverses, and more importantly under almost zero-voltage conditions. Thus, turn-on losses are virtually eliminated. An added benefit of this mode of turn-on is the prevention of high voltage stresses, which occur in inductive circuits in the presence of diode reverse recovery effects.

To realize zero-voltage turn-off, purely capacitive snubbers are required. Moreover, the turn-off process must be initiated when the active device is carrying a certain minimum current, the value of which is dependent on the circuit inductance and snubber capacitance. As the current through the device falls, the remaining current is diverted to the snubber capacitor causing its voltage to rise in a resonant manner. To maintain almost zero-voltage across the device during its fall time, and hence virtually eliminate the turn-off losses, the device needs to be over-snubbed.

The necessary conditions at the instant of turn-on and turn-off dictate a certain phase relationship between the voltage and current as seen from the a.c. terminals of the input and output bridges. To

realize these conditions, each bridge must be operated such that an effective lagging load is seen by looking into the transformer from its a.c. terminals. These constraints, which are crucial for realizing *soft-switching on all the devices of both the bridges* (and will be hence referred to as the *soft-switching constraints*), limit the region of operation on the Vout - Iout plane, as will be seen in the following analyses.

The primary objectives behind the analysis of each topology is :

1) to study the dependence of the output power, output voltage, transformer-kVA and filter capacitor-kVA on the control parameters

2) to identify the regions of operation, under soft-switching, on the Vout-Iout plane, and finally

3) to ascertain first-pass numbers on the kVA-ratings of the transformer and filter elements and device stresses at the given specifications, under optimum operating conditions for each topology. This gives a basis for comparing the three topologies.

To simplify the analysis the following assumptions are made with regard to each component of the proposed circuits :

The Switching Device :

1) Forward drop across the transistor or its antiparallel diode is zero.

2) The switching speed of the transistor/diode is infinite.

3) The diode has no reverse recovery effect.

The Transformer :

1) Negligible winding resistance as compared to the leakage reactance at the high switching frequencies of interest.

2) Infinite magnetizing inductance.

The Filter Capacitors :

1) Infinite capacitance, hence can be modelled as voltage sources.

2) Zero Effective Series Resistance (ESR).

3) Zero Effective Series Inductance (ESL).

The Snubber Capacitors :

1) The influence of the snubber capacitors on the voltage and current at the transformer terminals is ignored. This is justifiable, for this analysis, since it only comes into play during the switching transitions, which is substantially smaller than the switching period.

The influence of second order effects, namely finite device losses, finite magnetizing inductance of the transformer and the minimum current constraint at initiation of turn-off of the active

devices, on the limits of the desired region of operation are considered in subsequent chapters.

3.2 Single-Phase Single Active Bridge DC/DC Converter

Fig. 3.2.1(a) shows the idealized circuit schematic of Topology A. It consists of a dc voltage source followed by a capacitive filter feeding into a single-phase input active bridge, which serves as the dc to high frequency inverter. The input filter eliminates the undesirable high frequency current components generated by the switching action of the inverter. A transformer interfaces the inverter to the output diode rectifier bridge with a capacitive filter on its output side. Again, the purpose of the output filter is the same as that of the input. Conceptually, the entire circuit can be viewed as a voltage source interfaced to another voltage source through an inductor essentially the transformer modelled by its leakage inductance. The idealized primary-referred equivalent circuit is shown in Fig. 3.2.1(b) (snubber capacitance is set to zero, and magnetizing inductance to infinity). L is the total leakage inductance referred to the primary side.

The output dc voltage, and hence the output power, can be controlled by controlling the primary voltage of the transformer. To achieve this the two poles of the input bridge are phase shifted from each other by an angle β. Fig. 3.2.2a shows the ideal operating

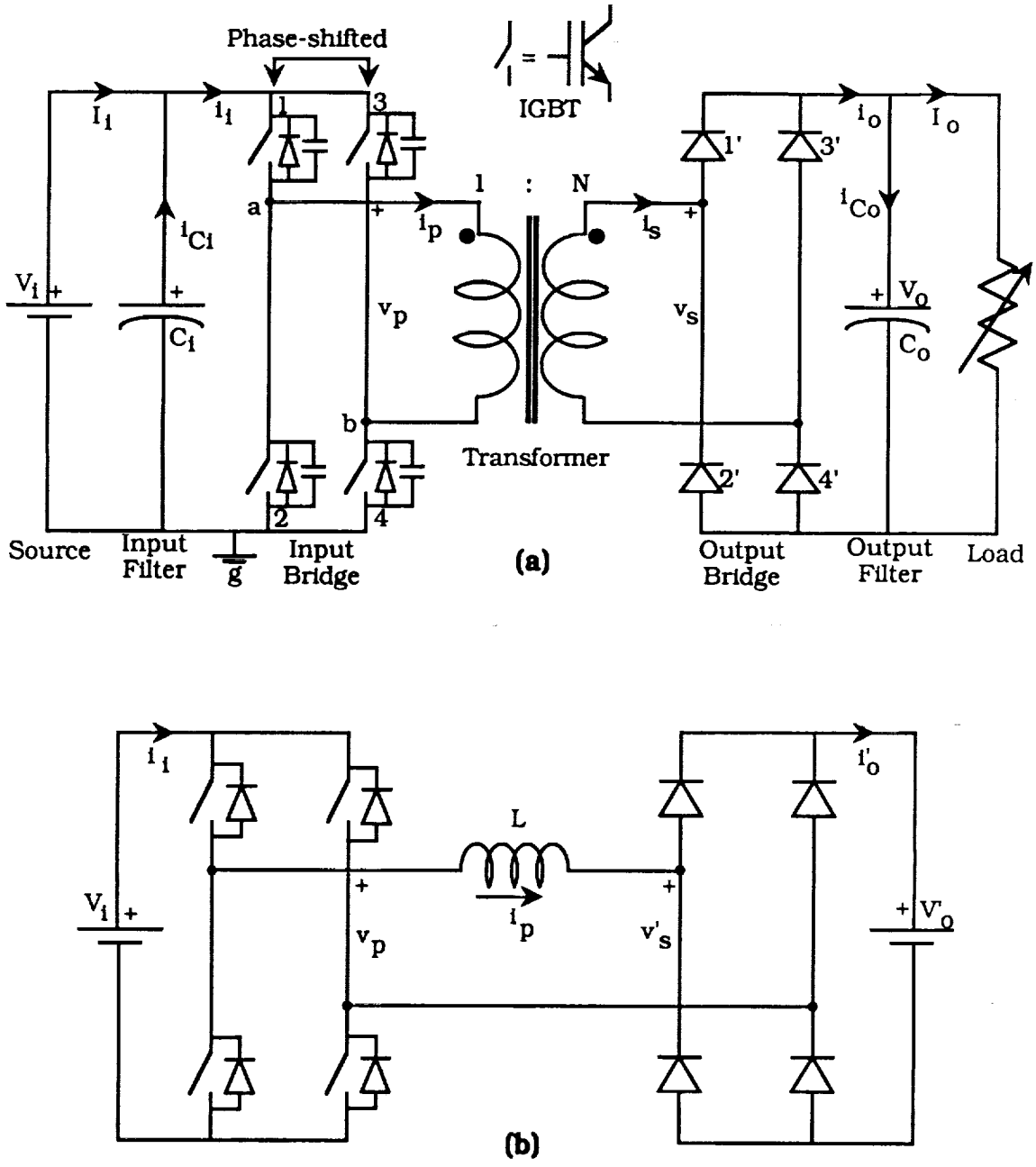


Fig. 3.2.1 (a) Circuit schematic of Single Phase Single Active Bridge DC/DC Converter (Topology A). (b) Ideal primary-referred equivalent circuit of Topology A.

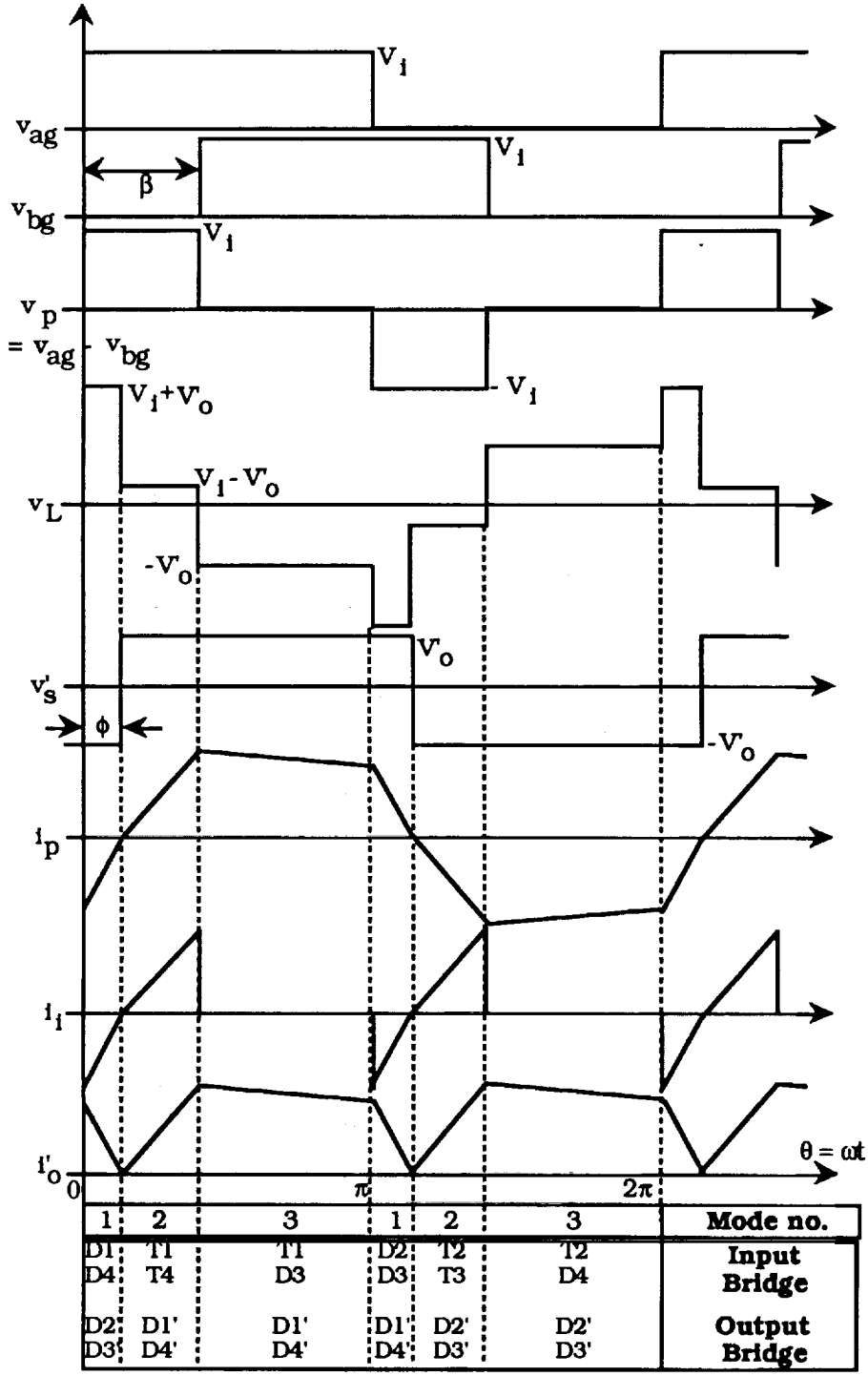


Fig. 3.2.2 (a) Ideal operating waveforms for Topology A under continuous conduction

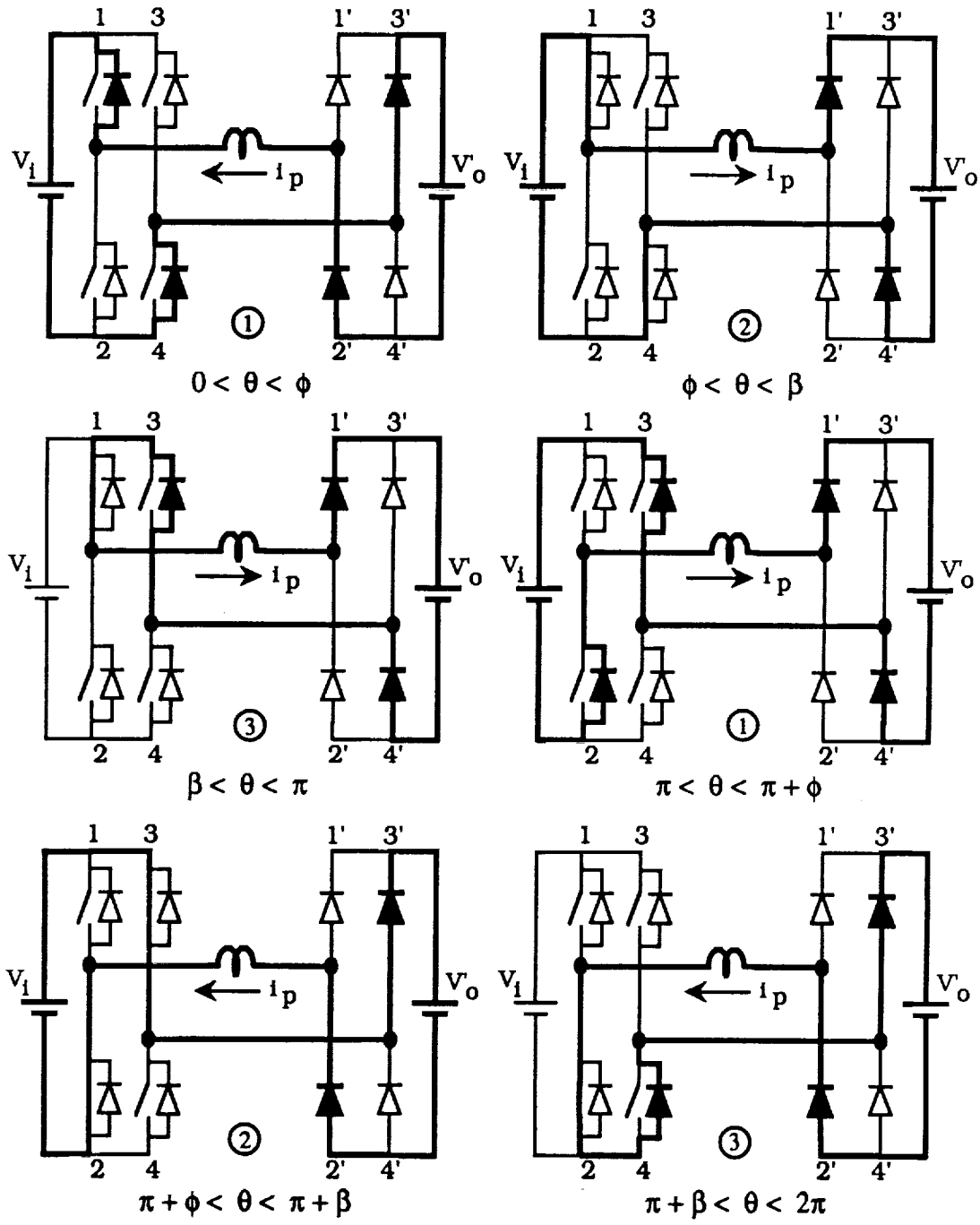


Fig. 3.2.2 (b) Six circuit modes of operation, under continuous conduction (Topology A).

waveforms. v_{ag} and v_{bg} are the pole voltages, and v_p, which is the difference in the two pole voltages, is applied across the primary winding of the transformer. Moreover, since the output diode bridge is current driven, the following constraints must be satisfied :

(i) When i_p is positive , v_s' must be positive(= V_o')

(ii) When i_p is negative, v_s' must be negative(= $-V_o'$)

Three modes of operation (for each half of the switching cycle) under continuous conduction case are identified. The six circuit modes are shown in Fig. 3.2.2b. This circuit enters discontinuous conduction mode under lightly loaded conditions, when the current in the input device reaches zero prior to its turn-off, at which point the device naturally commutates (zero-current switching). However, the incoming device experiences its snubber discharge, incurring substantial turn-on switching losses. As stated earlier, for zero-voltage switching (at turn-on and turn-off), the device must be carrying a minimum current at turn-off to allow transfer of energy from the snubber capacitor of the incoming device to that of the device turning-off. Hence, as seen, the discontinuous conduction mode of operation exhibits hard-switched turn-on of the devices. Discontinuous conduction is not analyzed, but it is important to keep in mind the restriction this imposes on the minimum load for achieving soft-switching on the active devices. In each mode, the

inductor current, ip as a function of $\theta = \omega t$, where ω is the switching frequency,is given by,

$$i_p(\theta) = \frac{[v_p(\theta) - v_s'(\theta)]}{\omega L}(\theta - \theta_i) + i_p(\theta_i) \qquad \theta_i \le \theta < \theta_f \qquad ...(3.2.1)$$

where, θ_i and θ_f are the start and end of each mode respectively, and $i_p(\theta_i)$ is the initial current of each mode. Therefore, from Fig. 3.2.2(a), (b) and eqn. (3.2.1),

Mode 1 : $0 \le \theta < \phi$; $\quad v_p(\theta) = V_i$; $v_s'(\theta) = -V_o'$

$$i_p(\theta) = \frac{V_i + V_o'}{\omega L}(\theta) + i_p(0) \qquad ...(3.2.2)$$

Mode 2 : $\phi \le \theta < \beta$; $\quad v_p(\theta) = V_i$; $v_s'(\theta) = V_o'$

$$i_p(\theta) = \frac{V_i - V_o'}{\omega L}(\theta - \phi) + i_p(\phi) \qquad ...(3.2.3)$$

Mode 3 : $\beta \le \theta < \pi$; $\quad v_p(\theta) = 0$; $v_s'(\theta) = V_o'$

$$i_p(\theta) = \frac{-V_o'}{\omega L}(\theta - \beta) + i_p(\beta) \qquad ...(3.2.4)$$

At the end of the half cycle, from symmetry conditions,

$$i_p(\pi) = -i_p(0) \qquad ...(3.2.5)$$

Hence, solving for $i_p(0)$, the complete current waveform can be obtained. From eqns. (3.2.2) - (3.2.5),

$$i_p(0) = \frac{V_o' (\pi - 2\phi) - V_i \beta}{2\omega L} \qquad \ldots(3.2.6)$$

From the soft-switching constraints, which require that the active device be conducting at turn-off, we get,

$$i_p(0) \leq 0$$

This, in turn, implies that,

$$\phi \geq 0 \qquad \ldots(3.2.7)$$

Further, from the output diode bridge constraints,

$$i_p(\phi) = 0$$

But, from Mode 1, at $\theta = \phi$,

$$i_p(\phi) = \frac{V_i + V_o'}{\omega L}(\phi) + i_p(0) = 0$$

Hence,

$$i_p(0) = - \frac{V_i + V_o'}{\omega L} (\phi) \qquad \ldots(3.2.8)$$

Therefore, equating the right-hand sides of eqns. (3.2.6) and (3.2.8), we get,

$$\phi = \frac{1}{2} (\beta - d\pi) \qquad \ldots(3.2.9)$$

where,

$$d = \frac{V_o'}{V_i} \qquad \ldots(3.2.10)$$

The parameter d represents the primary-referred dc voltage gain of the converter, often referred to as the dc conversion ratio. Comparing eqns. (3.2.7) and (3.2.9),

$$\beta - d\pi \geq 0$$

or,

$$d \leq \frac{\beta}{\pi}$$

Moreover, the diode bridge on the output restricts the minimum value of the output voltage to zero. Hence,

$$d \geq 0$$

Combining the above two constraints,

$$0 \leq d \leq \frac{\beta}{\pi} \qquad \ldots(3.2.11)$$

Bearing in mind the symmetrical manner in which the input and output bridges operate, the variation of β over the range 0 to π covers the entire operating region allowing soft-switching. Hence, theoretically, the maximum value of d obtainable is 1, as given by the above constraint relation. However, no power can be transferred under these conditions, since the resultant phase-shift, ϕ, from eqn. (3.2.9), between the two bridges is zero.

From a knowledge of $i_p(\theta)$ and the input and output converter switching functions, the steady state operating characteristics of the various quantities of interest, viz. output power, filter-kVA and transformer-kVA over the control parameter, β, and d are derived. Each of these quantities have been normalized to the following base:

Voltage base, $V_b = V_i$ ...(3.2.12a)

Current base, $I_b = \frac{V_i}{\omega L}$ ...(3.2.12b)

Power base, $P_b = V_b * I_b = \frac{V_i^2}{\omega L}$ ...(3.2.12c)

Moreover, since all the voltages and currents are referred to the primary side of the transformer the turns ratio must be taken into account to get the actual output quantities. For instance, $V_o = NV_o'$, $i_o = i_o' / N$, where N is the turns ratio of the transformer.

Output Power :

$$P_o = V_i I_i = V_o' I_o'$$

where, I_i (I_o) is the input (output) average current. Now,

$$I_i = \frac{1}{2\pi}\left[(\phi) i_p(0) + (\beta - \phi) i_p(\beta)\right]$$

$$= \left[\frac{V_i}{\omega L}\right] \frac{d}{4} \left[2\beta - \pi d^2 - \frac{\beta^2}{\pi} \right] \qquad ..(3.2.13a)$$

Hence,

$$P_o = \left[\frac{V_i^2}{\omega L}\right] \frac{d}{4} \left[2\beta - \pi d^2 - \frac{\beta^2}{\pi} \right] \qquad ...(3.2.13b)$$

To ascertain the absolute maximum power transfer point, the output power is first partially differentiated with respect to β, keeping d constant. Hence,

$$\frac{\partial P_o}{\partial \beta} = \left[\frac{V_i^2}{\omega L}\right] \frac{d}{4} \left[2 - \frac{2\beta}{\pi} \right] = 0$$

This gives us a very convenient result that for any d (within the permissible range), maximum power can be transferred at $\beta = \pi$. Of course, to ensure that this is the maximum power condition, one must verify that the second derivative of output power with respect to β is less than zero at $\beta = \pi$. This is seen to be true.

Now, to find the absolute maximum power transfer point for the converter, the output power can now be differentiated w.r.t. d after setting $\beta = \pi$. Hence,

$$\frac{dP_o}{dd} = \left[\frac{V_i^2}{\omega L}\right]\frac{\pi}{4}\left[1 - 3d^2\right] = 0$$

or,

$$d \approx 0.58$$

Thus, d = 0.58 and $\beta = \pi$ gives the absolute maximum power transfer point.

Fig. 3.2.3 shows the variation of output power, P_o, as a function of the control variable, β, with d as a parameter. For each value of d the output power is shown over the soft-switching region. The locus of the minimum power for each d defines the soft-switching boundary, and corresponds to $d = \beta / \pi$. As d increases, the range of β over which soft-switching can be achieved, diminishes. The curve corresponding to d = 0.58 is shown. The absolute maximum power transfer point is also shown on this curve at $\beta = \pi$ (see point labelled X).

Transformer kVA :

$$T\_kVA = \frac{v_{prms} * i_{prms} + v'_{srms} * i'_{srms}}{2}$$

However, since magnetizing current is assumed zero,

$$T\_kVA = \frac{(v_{prms} + v'_{srms}) * i_{prms}}{2} \qquad \ldots(3.2.14a)$$

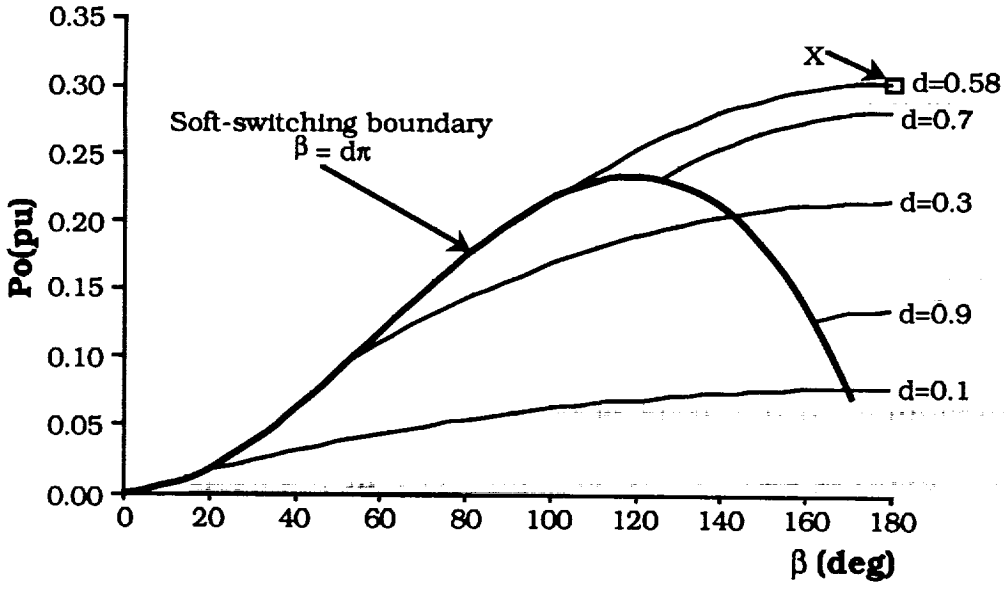


Fig. 3.2.3 Output Power, P_o, vs β with d as a parameter, under soft switching operation (Topology A).

where,

$$v_{prms} = V_i \sqrt{\frac{\beta}{\pi}}; \quad v'_{srms} = V'_o = d\, V_i$$

$$i_{prms} = \sqrt{\frac{1}{\pi} \int_0^{\pi} i_p^2 \, d\theta}$$

Define,

$$\text{Transformer Utilization} = \frac{P_o}{T\_kVA} \qquad \ldots(3.2.14b)$$

Fig. 3.2.4a shows the dependence of the transformer kVA on β and Fig. 3.2.4b shows its dependence on the output power. In each case a family of curves is plotted with d as the parameter. Again, the soft-switching regions are shown. The locus of the minimum kVA for each d defines the soft-switching boundary. Various design points can be selected based on issues of maximum power transfer capability or range of controllability under soft-switching. From Fig. 3.2.4b, it is seen that as one alternative, the transformer can be designed to handle the absolute maximum power of 0.302pu (which is shown on the curve corresponding to d = 0.58) for the minimum kVA. This gives a transformer kVA of 0.475pu and hence, a transformer utilization of 0.636. However, this restricts the range of

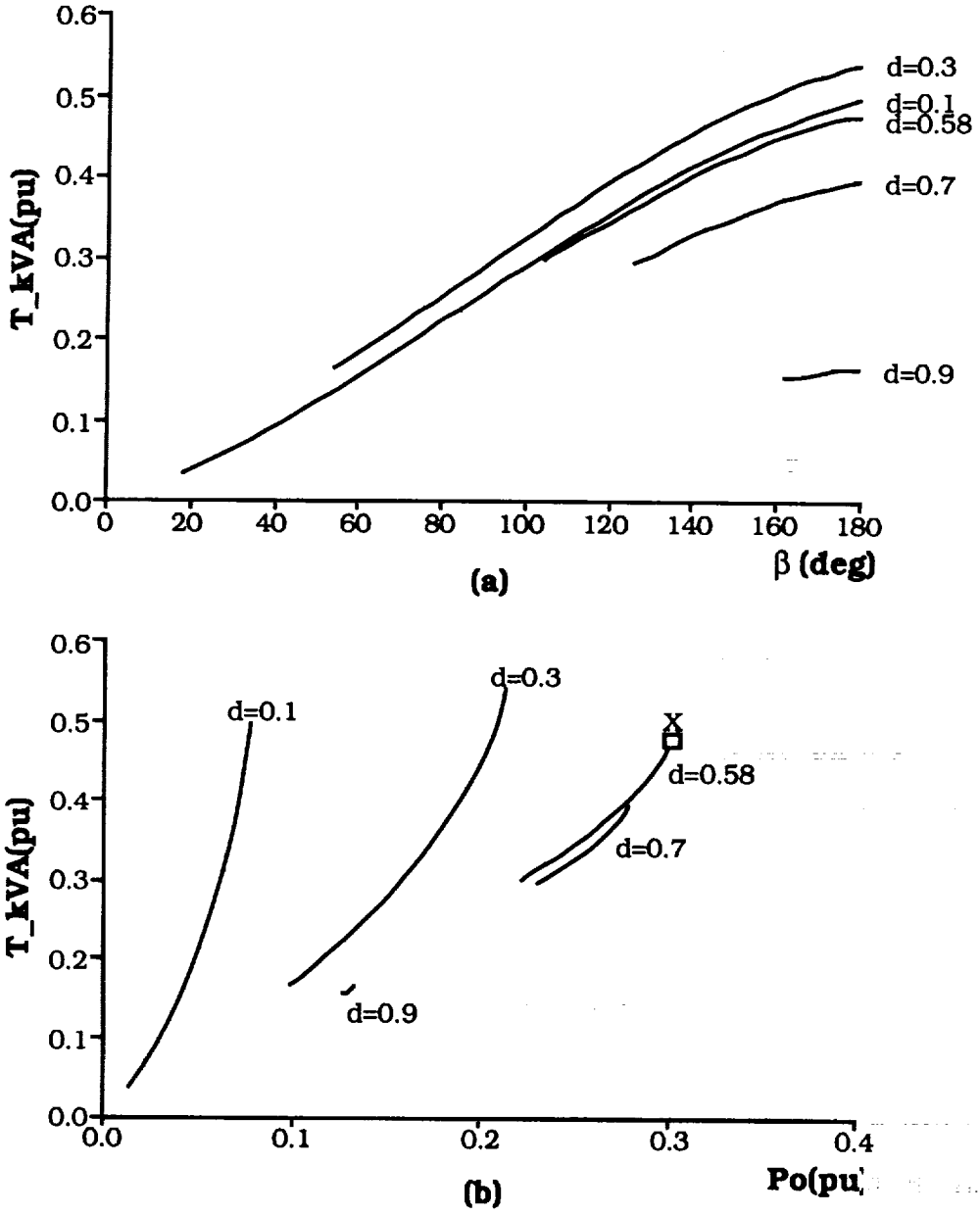


Fig. 3.2.4 (a) Transformer kVA vs β with d as a parameter, under soft switching operation (Topology A). (b) Transformer kVA vs P_o with d as a parameter, under soft switching operation (Topology A)

control upto a point where the transformer kVA cannot exceed the above value. On the other hand, for full range of control over β, the transformer would have to be designed for the maximum kVA required, which is approximately 0.55pu. However, under these conditions the best transformer utilization turns out to be 0.549, which is poorer than the first design. Thus, it is seen that a trade-off between size (and, hence, power density) and controllability must be made.

Input Filter Capacitor kVA :

$$Ci\_kVA = V_i^* \, i_{Cirms} \qquad \ldots(3.2.15)$$

where,

$$i_{Cirms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_i^2 \, d\theta - I_i^2}$$

Figs. 3.2.5a and 3.2.5b show the variation of the input filter capacitor kVA with β and output power, respectively, with d as the parameter. Each curve extends over the soft-switching region only. For a given d, as β increases, the capacitor kVA increases. This is because the harmonic (ripple) content of the current into the input converter increases. Again, it is seen from Fig. 3.2.5b that good controllability demands high kVA ratings on the input filter and,

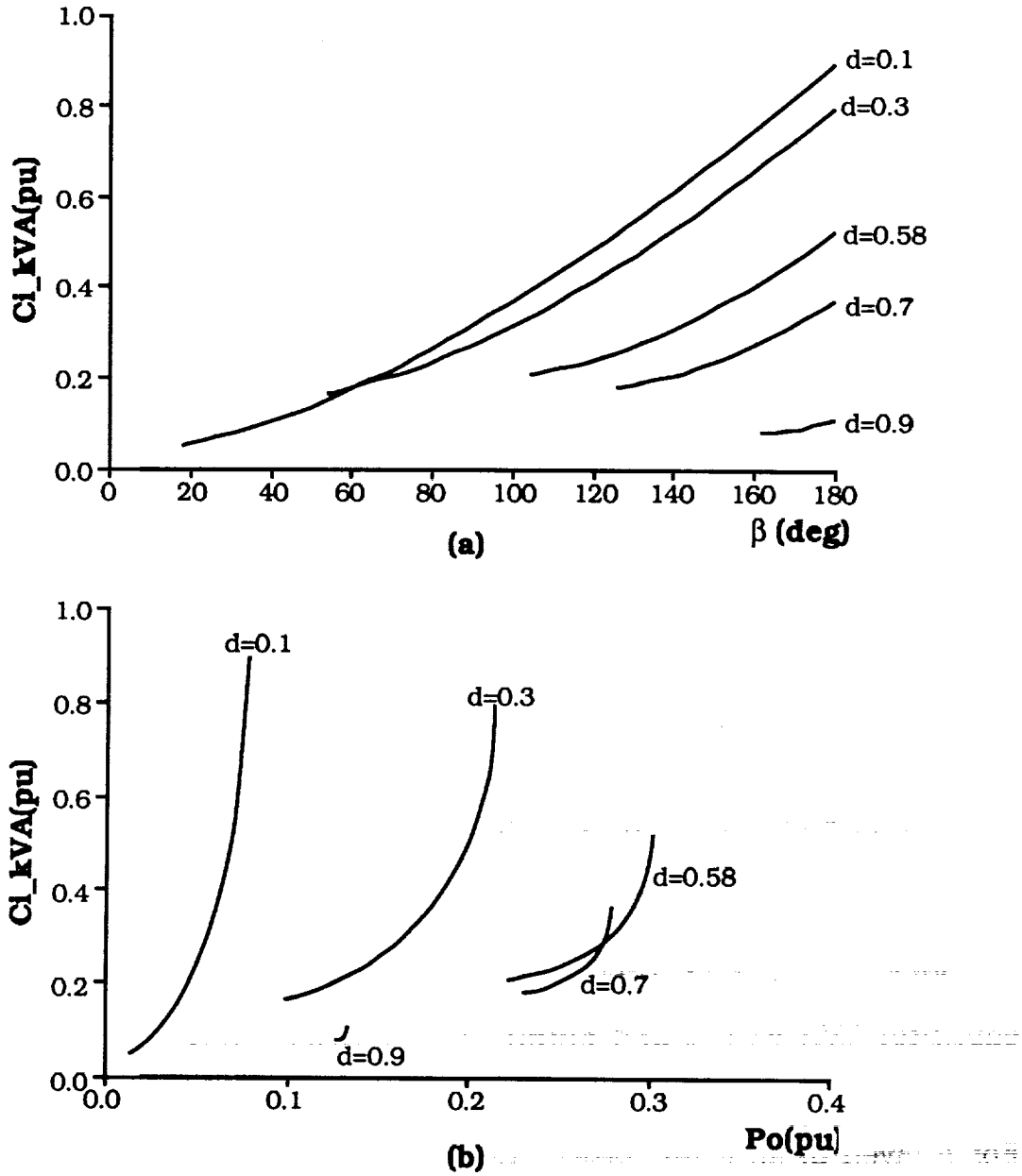


Fig. 3.2.5 (a) Input Filter Capacitor kVA vs β with d as a parameter, under soft switching operation. (b) Input Filter Capacitor kVA vs P_o with d as a parameter, under soft switching operation. (Topology A)

hence, bigger size. For maximum power transfer, only a certain minimum kVA is required which is a little more than half that required for full control. However, one loses on the range of control.

Output Filter Capacitor kVA :

$$Co\_kVA = V_o' * i_{Corms}' \qquad ...(3.2.16)$$

where,

$$i_{Corms}' = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_o'^2 \, d\theta - I_o'^2}$$

Figs. 3.2.6a and 3.2.6b show the variation of the output filter capacitor kVA with β and output power, respectively, with d as the parameter. Each curve extends over the soft-switching region only. The trend in the variation for a given d, as β increases, is similar to that of the input capacitor kVA. However, the worst case turns out to be for d = 0.58. Moreover, comparing the relative magnitudes of the kVAs required for the input and output capacitors, it is seen that, in general, over the entire operating region, the output capacitor kVA requirement is much lower. This is a consequence of the output bridge being a diode bridge, and hence restricting the output current to be unidirectional only. Selection of the output capacitor, based on the minimum kVA required for maximum power transfer suffices, since this also allows full control.

Fig. 3.2.7 shows the entire region of soft-switching on a V_o' - I'_o plane. For higher output voltages, the load range becomes smaller. A more detailed discussion on this plot will be presented in the subsequent chapter on the comparison of the proposed topologies.

Another quantity of paramount concern is the peak current stresses in the switching devices. The peak current occurs at $\theta = \beta$, and is given as,

$$i_{pk} = \frac{V_i}{2\omega L} (1 - d) (\beta + d\pi) \qquad ...(3.2.17)$$

Knowledge of the absolute peak current, given by the above equation, is essential for proper rating and selection of the devices. Moreover, the switching and conduction losses are strongly dependent on the peak current. However, more information on the device utilization and converter characteristics is obtained from the ratio of the peak current to the average current. From eqns. (3.2.13a) and (3.2.17),

$$\frac{i_{pk}}{I_i} = \frac{2\pi (1 - d) (\beta + d\pi)}{d (2\pi\beta - \pi d^2 - \beta^2)} \qquad ...(3.2.18)$$

A typical problem with such converters is the huge inrush currents at start-up, when the output voltage is very low. To maintain the peak currents at a minimum during start-up, the above equation can be differentiated w.r.t. to β and set to zero to give the following control law,

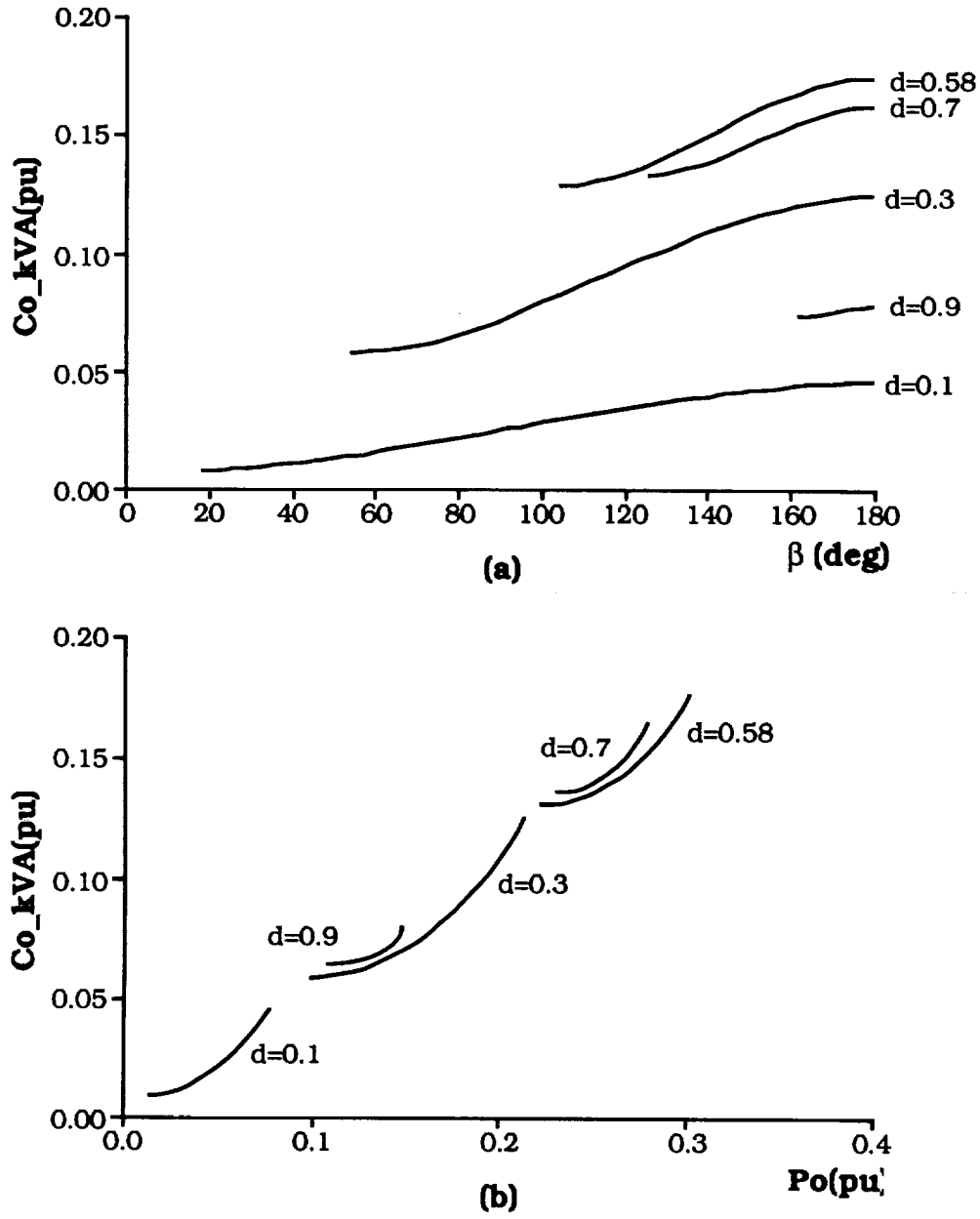


Fig. 3.2.6 (a) Output Filter Capacitor kVA vs β with d as a parameter, under soft switching operation. (b) Output Filter Capacitor kVA vs P_o with d as a parameter, under soft switching operation. (Topology A)

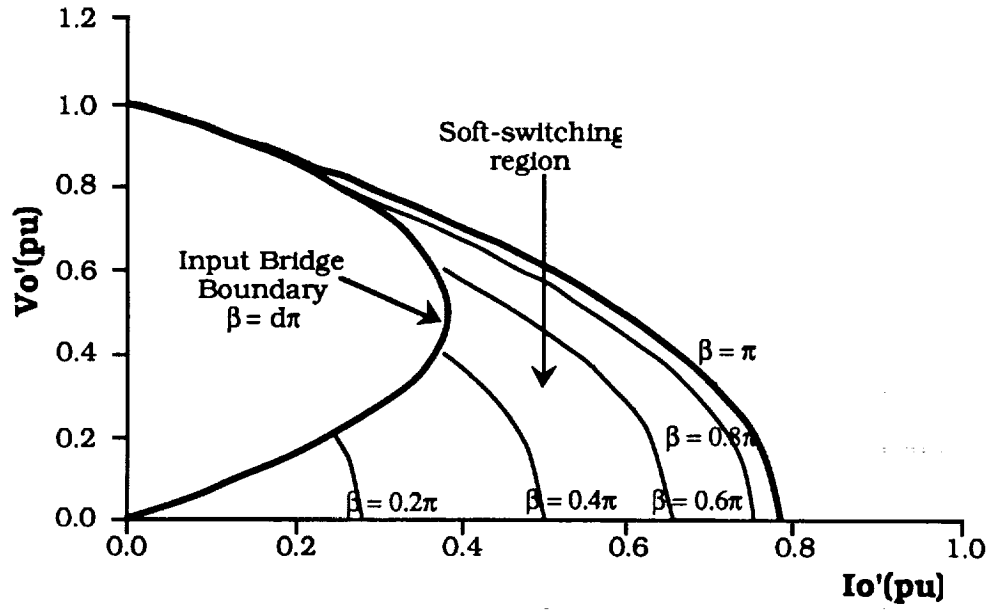


Fig. 3.2.7 Output Voltage vs Output Current, showing constant β-lines in the soft switching region of operation. (Topology A)

$$\beta = \left[- d + \sqrt{2(d + d^2)} \right] \pi \qquad \ldots(3.2.19)$$

Fig. 3.2.8a shows a plot of switch peak current (normalized to the input average current) as a function of β for different d's. As seen, for any β as d (output voltage) decreases peak current increases. Fig. 3.2.8b shows a plot of the above relation between β and d, to keep the switch peak current at a minimum during start-up (when the output voltage is building up). Such a control law could be implemented for a battery-charger application.

In practice, a major limitation on the operation of this converter is seen to arise from the reverse recovery effects of the output diodes. In brief, the phenomenon of diode reverse recovery is the removal of the stored charge on the junction capacitance during turn-off. The required peak reverse current is, thus, a function of the rate of fall of forward current through the diode (which is governed by the circuit inductance and switching period). Given the need for high switching frequency (for high power density) and reasonably low leakage inductance, one could expect very high peak reverse currents. Now, a fast recovery diode, would lead to very high voltage stresses on the circuit elements owing to the fact that a large current (reverse diode current) flowing through the leakage inductance is 'snapped off'. On the other hand, a slow recovery diode would impose an upper limit on the switching frequency. These considerations force a designer to make certain trade-offs, which at

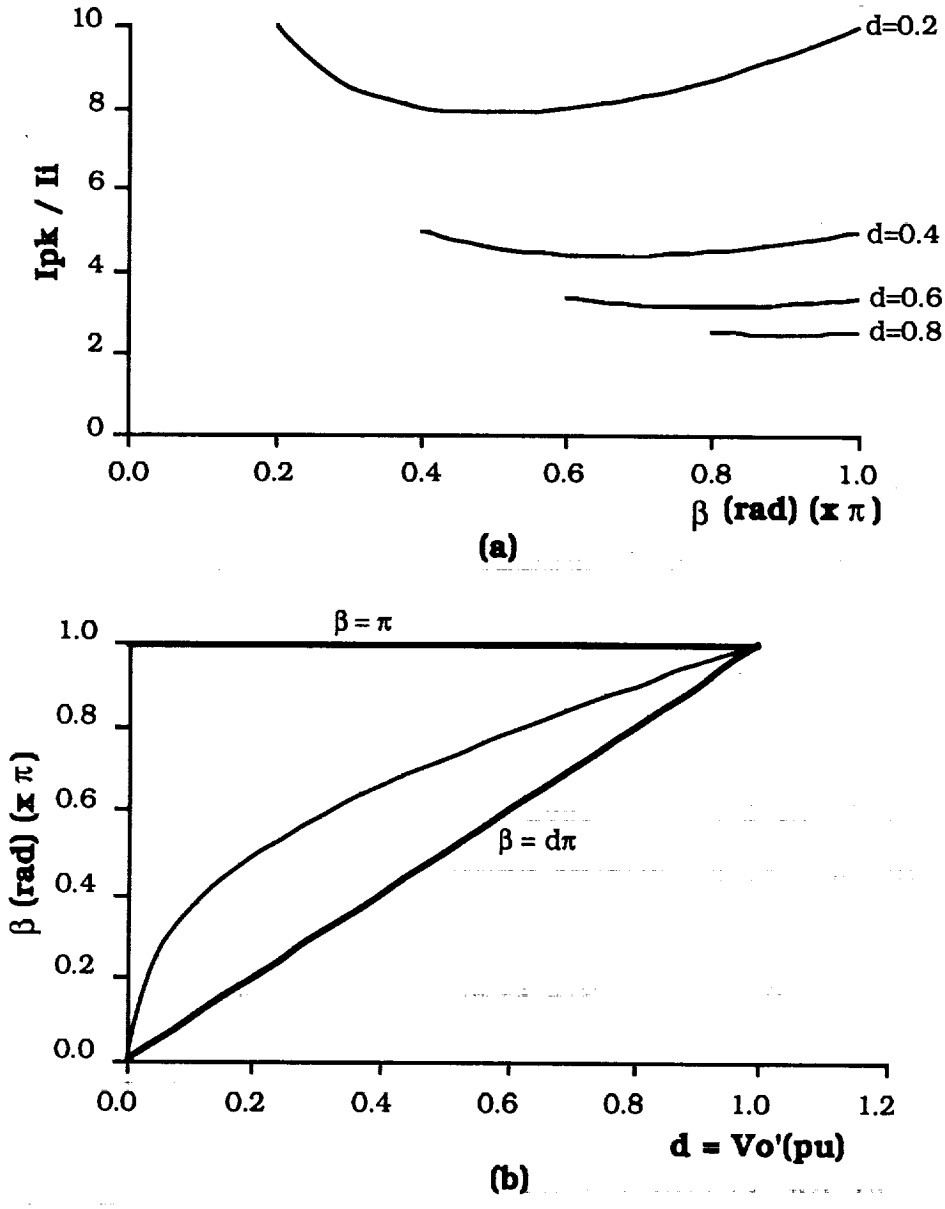


Fig. 3.2.8 (a)Plot of peak device current(as a ratio of average current) versus β for different d's. (b)Plot of the control law governing β as a function of output voltage to keep peak device current at a minimum (Topology A)

times inhibits one from exploiting the full capabilities of a circuit.

However, as reported in Reference [20], the diode recovery process is conceptually akin to the existence of an active device in anti-parallel to the diode. Recalling the soft-switching constraint that the active device must take over conduction from its anti-parallel diode, it follows that if the output diodes are now replaced by switching devices (active device with anti-parallel diode) then the output bridge also naturally (and most importantly benignly) handles the diode reverse recovery process. The circuit can now be operated with a simpler control strategy in which the input and output bridges generate square waves phase-shifted from each other. Also, all the active devices of both the bridges can operate under soft-switching conditions. Two quadrant operation is also realizable. The following section analyzes this new topology.

3.3 Single-Phase Dual Active Bridge DC/DC Converter

Fig. 3.3.1(a) shows the circuit schematic of Topology B. It is similar to Topology A except the output diode bridge has been replaced by an active bridge, and hence the name. The leakage inductance of the transformer is, again, used as the main energy transfer element from the input to the output. The primary-referred equivalent circuit is shown in Fig. 3.3.1(b). L is the total leakage inductance referred to the primary side.

The output dc voltage, and hence the output power, can now be controlled by controlling the phase shift, ϕ, between the two active bridges. Both the bridges operate as simple square wave inverters, as viewed from their dc sides, switching at a constant frequency. However, by phase-shifting the square waves the effective voltage across the leakage inductance and hence the current can be controlled. Net power flows from the leading bridge to the lagging bridge. Fig. 3.3.2 shows the operating waveforms for the case where the square wave generated by the input bridge leads that of the output bridge. The input bridge current, leakage inductance current and output bridge current are shown for three different dc conversion ratios (buck, unity and boost).

Two modes of operation (for each half cycle) can be identified. In each mode, the inductor current, i_p as a function of $\theta = \omega t$, where ω is the switching frequency, is given by,

$$i_p(\theta) = \frac{[v_p(\theta) - v_s'(\theta)]}{\omega L}(\theta - \theta_i) + i_p(\theta_i) \qquad \theta_i \le \theta < \theta_f$$

...(3.3.1)

where, θ_i and θ_f are the start and end of each mode respectively, and $i_p(\theta_i)$ is the initial current of each mode. Therefore, from Fig. 3.3.2 and eqn. (3.3.1),

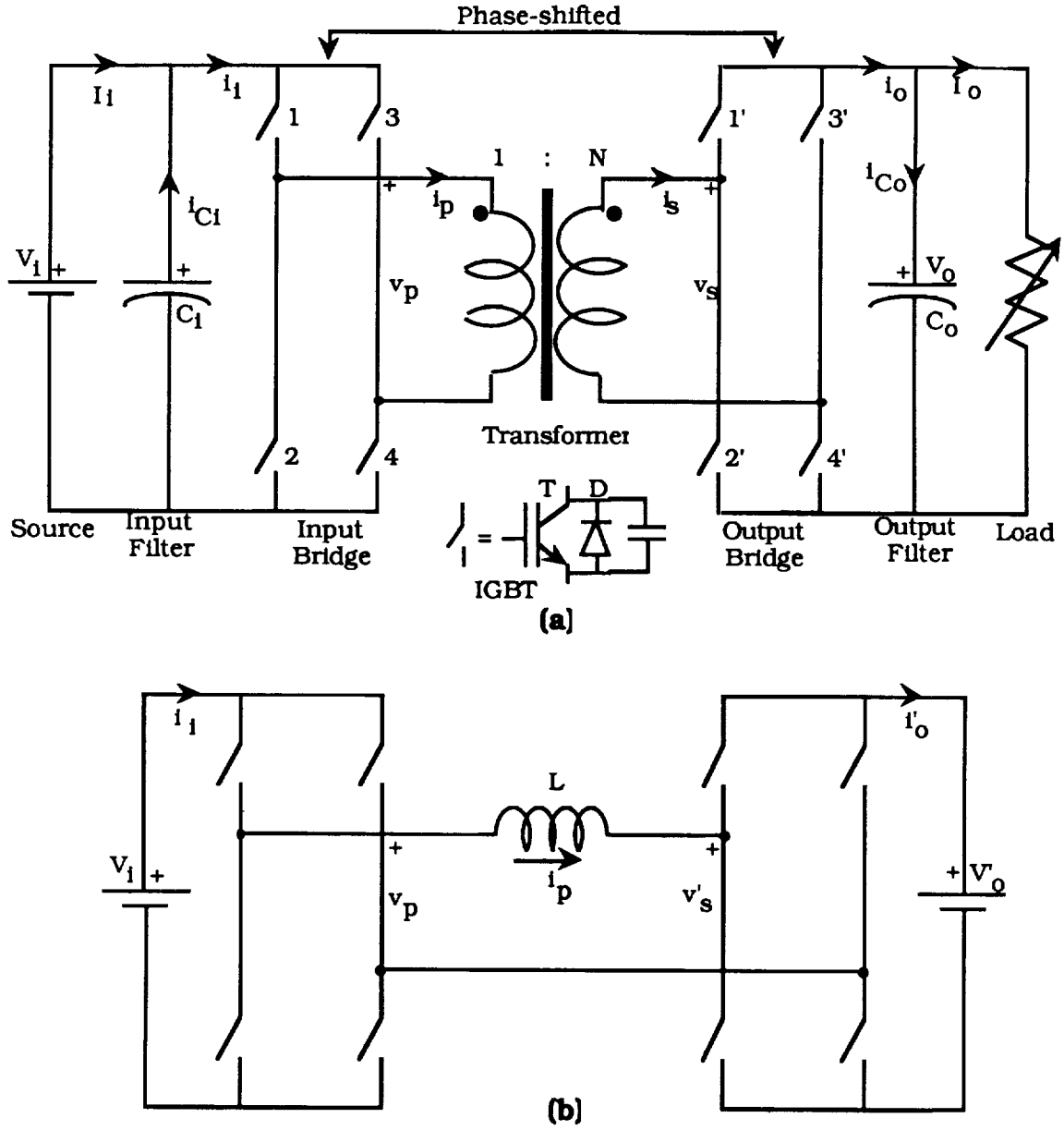
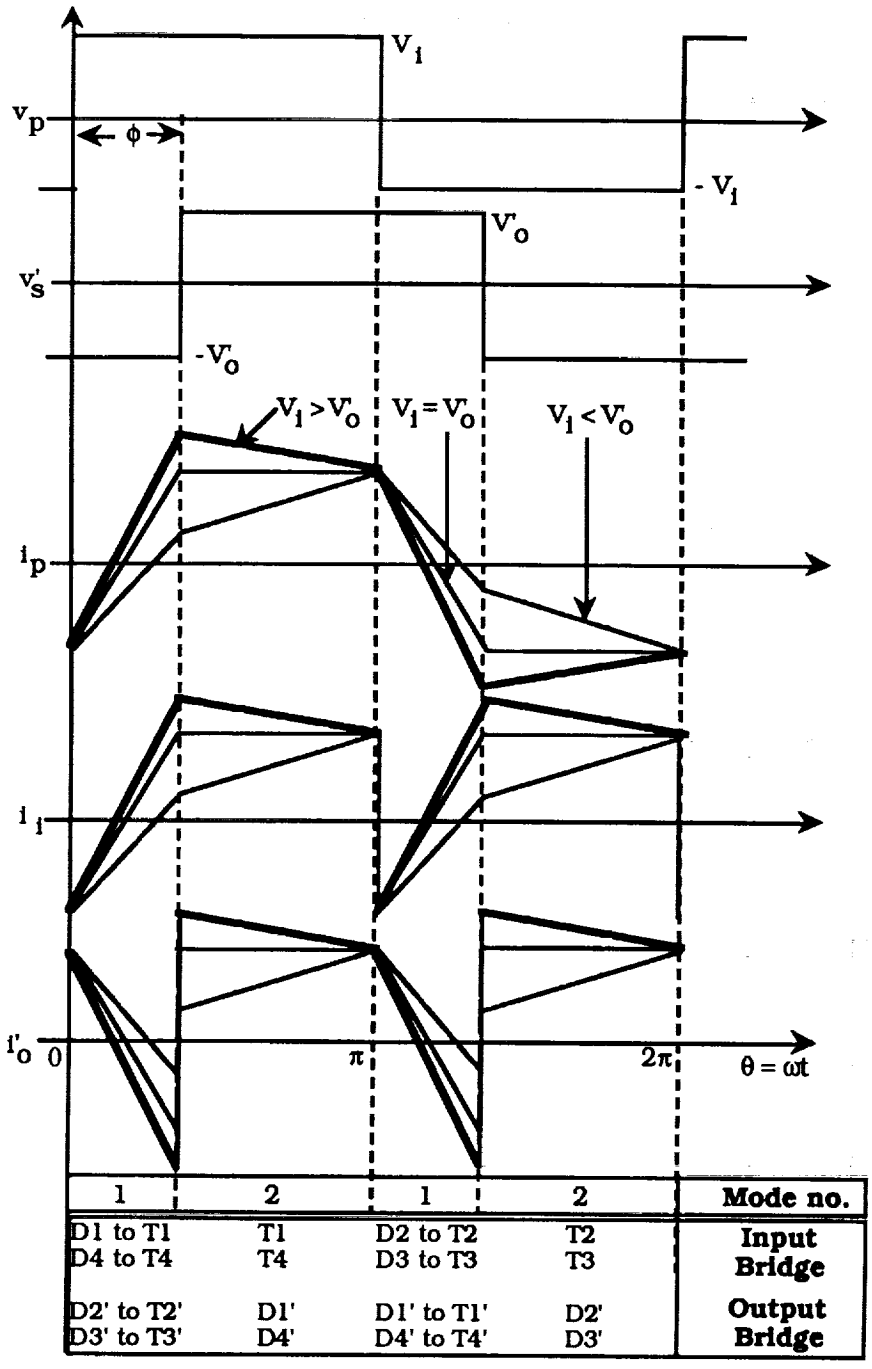


Fig. 3.3.1 (a) Circuit schematic of Single Phase Dual Active Bridge DC/DC Converter (Topology B). (b) Primary referred equivalent circuit.



1	2	1	2	Mode no.
D1 to T1 D4 to T4	T1 T4	D2 to T2 D3 to T3	T2 T3	Input Bridge
D2' to T2' D3' to T3'	D1' D4'	D1' to T1' D4' to T4'	D2' D3'	Output Bridge

Fig. 3.3.2 Ideal operating waveforms for Topology B. Input bridge is leading the output bridge.

Mode 1 : $0 \le \theta < \phi$; $v_p(\theta) = V_i$; $v_s'(\theta) = -V_o'$

$$i_p(\theta) = \frac{V_i + V_o'}{\omega L}(\theta) + i_p(0) \qquad ...(3.3.2)$$

Mode 2 : $\phi \le \theta < \pi$; $v_p(\theta) = V_i$; $v_s'(\theta) = V_o'$

$$i_p(\theta) = \frac{V_i - V_o'}{\omega L}(\theta - \phi) + i_p(\phi) \qquad ...(3.3.3)$$

At the end of the half cycle, from symmetry conditions,

$$i_p(\pi) = -i_p(0) \qquad ...(3.3.4)$$

Hence, solving for $i_p(0)$, the complete current waveform can be obtained. From eqns. (3.3.2) - (3.3.4),

$$i_p(0) = \frac{-V_i}{\omega L}\left[d\phi + \frac{\pi(1 - d)}{2}\right] \qquad ...(3.3.5)$$

Also,

$$i_p(\phi) = \frac{-V_i}{\omega L}\left[-\phi + \frac{\pi(1 - d)}{2}\right] \qquad ...(3.3.6)$$

where,

$$d = \frac{V_o'}{V_i}$$

From the soft-switching constraints we get,

For Leading (Input) Bridge $i_p(0) \le 0$

therefore, substituting this in eqn. (3.3.5),

$$d \leq \frac{1}{1 - \frac{2\phi}{\pi}} \qquad 0 \leq \phi < \frac{\pi}{2} \qquad \ldots(3.3.7)$$

For Lagging (Output) Bridge $i_p(\phi) \geq 0$

therefore, substituting in eqn.(3.3.6),

$$d \geq \frac{\pi - 2\phi}{\pi} \qquad 0 \leq \phi < \frac{\pi}{2} \qquad \ldots(3.3.8)$$

Also, the anti-parallel diodes demand

$$d \geq 0 \qquad \ldots(3.3.9)$$

Note, constraints (3.3.7) and (3.3.8) must be used in conjunction with constraint (3.3.9). Violating the leading(input) bridge constraint results in natural commutation of all its active devices. In other words, the device turns off when the current through it naturally reverses. This is undesirable, since the incoming active device turns on discharging its snubber capacitor and thus resulting in substantial turn-on losses. This is commonly referred to as a 'snubber dump'. Similarly, violating the lagging (output) bridge constraint leads to natural commutation of all its active devices. The boundary represents diode bridge operation and is identical to that for Topology A, when $\beta = \pi$. The output bridge constraint will be referred to as the diode bridge constraint. The two boundaries enclose the region of soft-switching. Moreover, from eqn. (3.3.7), d

can be greater than unity, that is, this topology can also operate as a boost converter.

Theoretically, from eqn. (3.3.7) at $\phi = \pi / 2$, d can tend to infinity. In a real circuit the voltage gain is limited by losses. For $\pi > \phi > \pi / 2$, soft-switching of the active devices is still achievable for any d. However, the power transferred is reduced, with a substantial energy circulating in the filter capacitors.

Given the symmetry of the circuit, a similar analysis for $0 \geq \phi > -\pi/2$ was carried out. The square wave generated by the output bridge now leads that of the input bridge. The directions of input and output average currents are reversed, and hence, power flow is reversed. More importantly, this reversal of power flow is also possible within soft-switching boundaries identical to those for the range $0 \leq \phi < \pi / 2$. The expression for average output power, derived below, is valid for both directions of power flow. For positive ϕ (input bridge leading the output bridge) net power flows from the input bridge to the output bridge (forward flow), and for negative ϕ (input bridge lagging the output bridge) net power flows from the output bridge to the input bridge (reverse flow).

With a knowledge of the primary current, $i_p(\theta)$, and the converter switching functions the various quantities of interest defined in the previous section are once again calculated, and are given below.

Output Power :

$$P_o = V_i I_i = V_o' I_o'$$

$$= \left[\frac{V_i^2}{\omega L}\right] d\,\phi \left[1 - \frac{|\phi|}{\pi}\right] \qquad -\pi/2 \le \phi \le \pi/2 \qquad \ldots(3.3.10)$$

For any d, maximum power transfer is achievable at $\phi = \pi / 2$.

Transformer kVA :

$$T\_kVA = \frac{v_{prms} * i_{prms} + v_{srms}' * i_{srms}'}{2}$$

However, since magnetizing current is assumed zero,

$$i_{prms} = i_{srms}'$$

Therefore,

$$T\_kVA = \frac{(v_{prms} + v_{srms}') * i_{prms}}{2} \qquad \ldots(3.3.11)$$

where,

$$v_{prms} = V_i; \qquad v_{srms}' = V_o' = d\,V_i$$

$$i_{prms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_p^2 \, d\theta}$$

All other quantities are calculated as defined in the previous section. The steady state operating characteristics of each quantity of interest, normalized to the same base as defined in the last section, are plotted as a function of the control variable, ϕ, with d as a parameter. The boundaries of soft-switching are also shown on these characteristics.

Two sets of output power characteristics versus ϕ, calculated from eqn. (3.3.10), are shown in Fig. 3.3.3. In Fig. 3.3.3a the parameter d sweeps from 0.2 to 1, with the control variable, ϕ, sweeping over the full allowable range of $-\pi / 2$ to $\pi / 2$. The soft-switching region for each value of d is identical in each quadrant. The d = 1 curve gives full control, under soft-switching. Fig. 3.3.3b shows the output power characteristics for $d > 1$ also. The soft-switching region is now enclosed within the two boundaries given by eqns. (3.3.7) and (3.3.8). For values of $d > 1$ or < 1, the range of ϕ for soft-switching is reduced. For any d maximum power transfer occurs at $\phi = \pi / 2$.

Fig. 3.3.4a shows the dependence of the transformer kVA on ϕ and Fig. 3.3.4b shows its dependence on the output power. In each case a family of curves is plotted with d as the parameter. Again, the

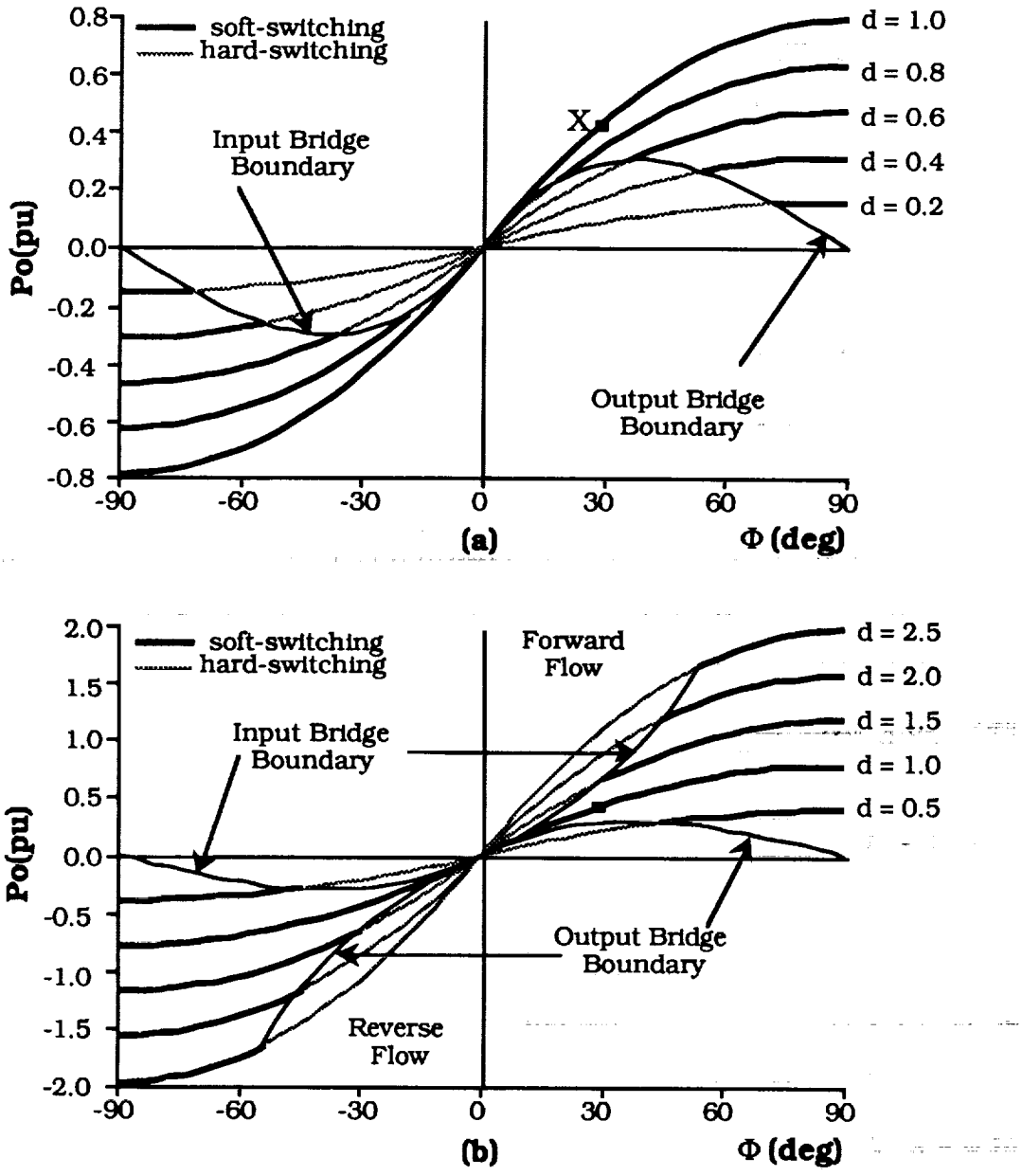


Fig. 3.3.3 (a) Output Power vs ϕ with d as a parameter, showing two quadrant operation. (b) Output Power vs ϕ with d as a parameter, showing two quadrant and buck-boost operation.(Topology B)

soft-switching regions are shown. Various design points can be selected based on issues of maximum power transfer capability or range of controllability under soft-switching. Fig. 3.3.4b shows the output bridge constraint (also, referred to as the diode bridge constraint). An interesting feature of Topology B can be brought to light, by examining the minimum transformer kVA (0.475pu) required for transferring the maximum output power (0.302pu) on the diode bridge constraint (which corresponds to the $\beta = \pi$ boundary for Topology A). For the same kVA the output power can be increased to 0.422pu at d = 1 (see point labelled X), with Topology B. This gives us a transformer utilization of 0.888, an improvement of 40%. However, this restricts the range of control upto a point where the transformer kVA cannot exceed the above value.

On the other hand, for full range of control over ϕ at d = 1, the transformer would have to be designed for the maximum kVA of approximately 1.3pu, resulting in a transformer utilization of 0.604. Thus, it is seen again that a trade-off between size (and, hence, power density) and controllability must be made.

One might wonder, and justifiably so, at this 40% improvement in the transformer utilization with Topology B. A possible explanation is that with the diode bridge at the output the transformer always sees a resistive load (on a fundamental component basis). Hence, maximum power transfer is governed by a passive impedance divider consisting of the leakage impedance and the resistive load. On the

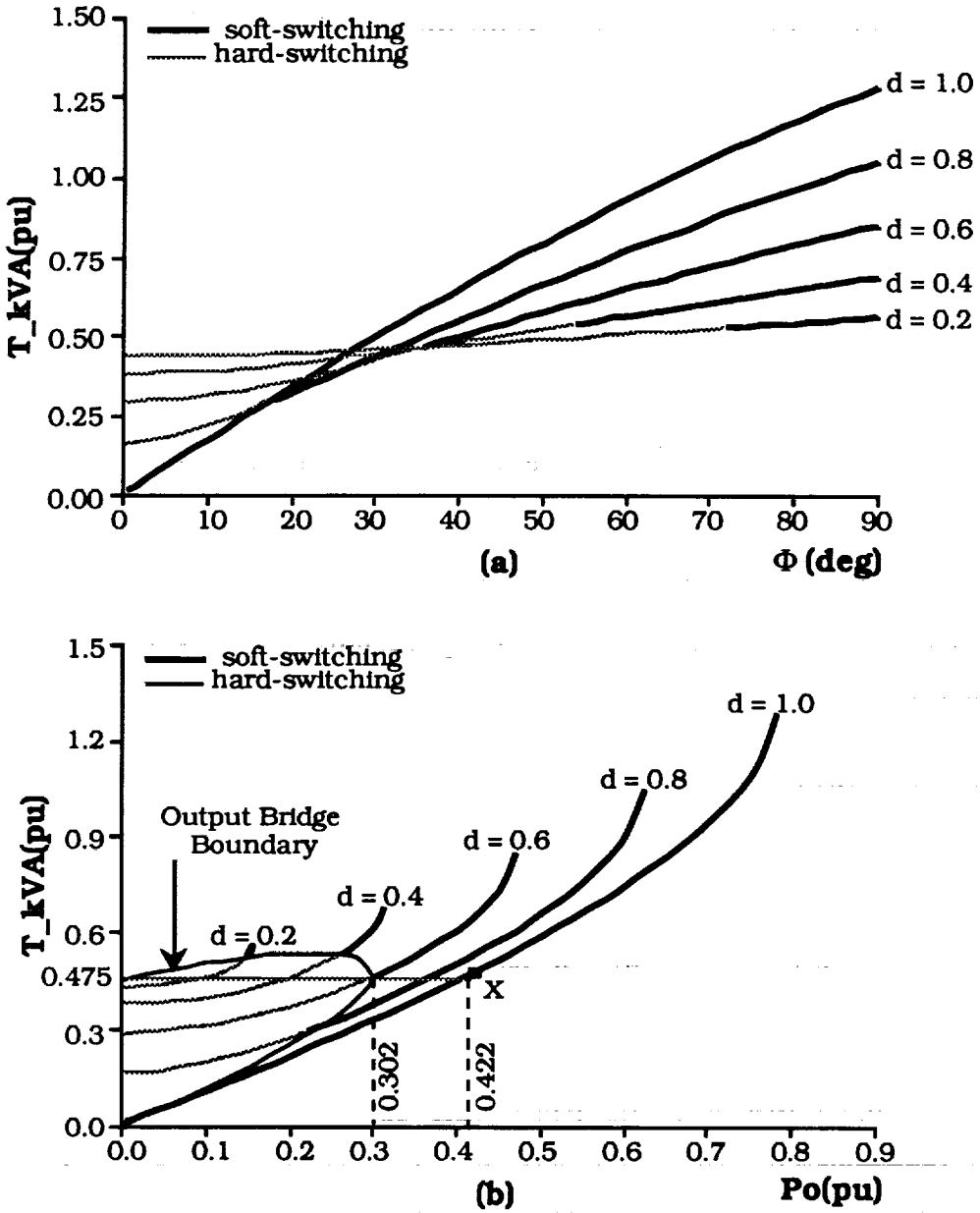


Fig. 3.3.4 (a) Transformer kVA vs ϕ with d as a parameter. (b) Transformer kVA vs P_o with d as a parameter. (Topology B)

other hand the active output bridge serves as a source of reactive excitation for the transformer. This allows more of the primary kVA supplied by the input bridge to be in the form of real output power.

Figs. 3.3.5a, b show the variation of the input capacitor kVA with ϕ and output power, respectively, for various values of d. For a wide range of ϕ the input capacitor kVA is seen to be a minimum at d = 1. Again, various design trade-offs can be made depending upon good range of controllability and high power density.

Figs. 3.3.6a, b show the dependence of the output filter capacitor on ϕ and output power, respectively, with d as the parameter. Contrary to the input filter capacitor, for a considerable range of ϕ, the output filter capacitor kVA is highest at d = 1.

Fig. 3.3.7 shows the entire region of soft-switching on a V_o' - I'_o plane. At d=1 (V_o' = 1pu), theoretically any load from no-load to the maximum limited by the vertical line (corresponding to $\phi = \pi/2$) can be realized.The range of load decreases on either side of d = 1. The boundaries and regions of soft-switching are identical in both directions of power flow.

Further comments on the merits and demerits of this topology are reserved till a later chapter, where a detailed comparison of the stresses in the three proposed topologies is presented.

For the sake of completeness, it is worth mentioning here that various other control strategies can be devised for Topology B. For

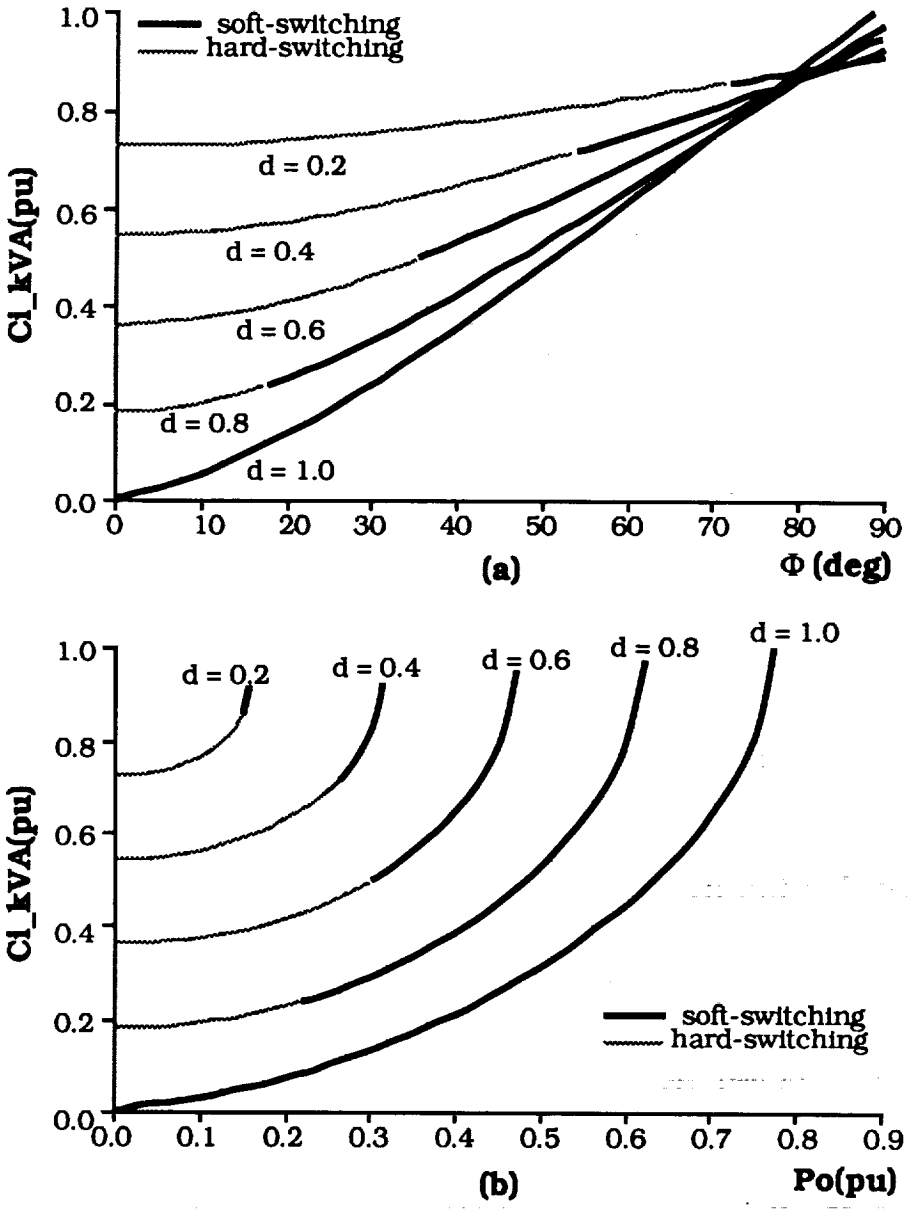


Fig. 3.3.5 (a) Input Filter Capacitor kVA vs ϕ with d as a parameter. (b) Input Filter Capacitor kVA vs P_o with d as a parameter. (Topology B)

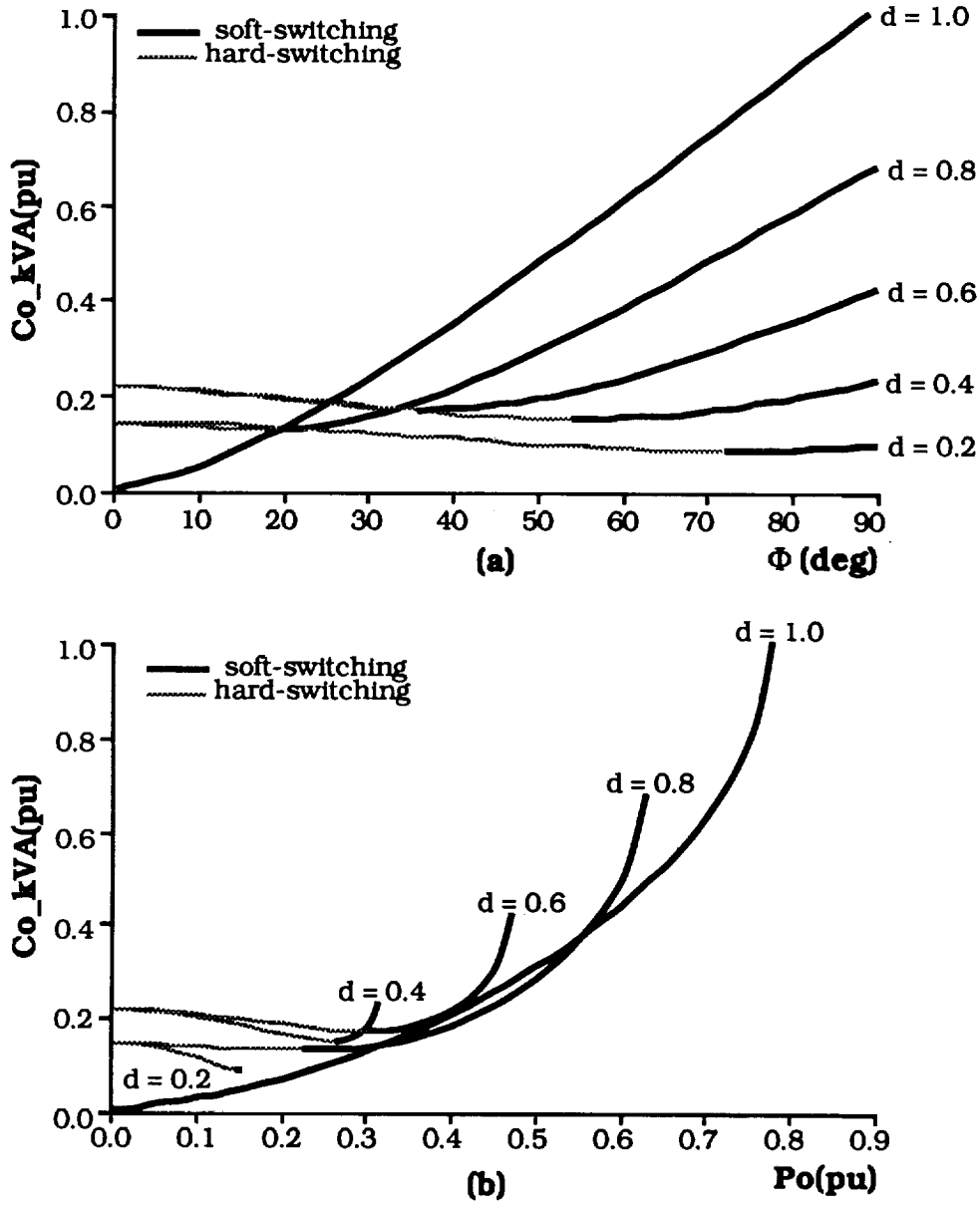


Fig. 3.3.6 (a) Output Filter Capacitor kVA vs ϕ with d as a parameter. (b) Output Filter Capacitor kVA vs P_o with d as a parameter. (Topology B)

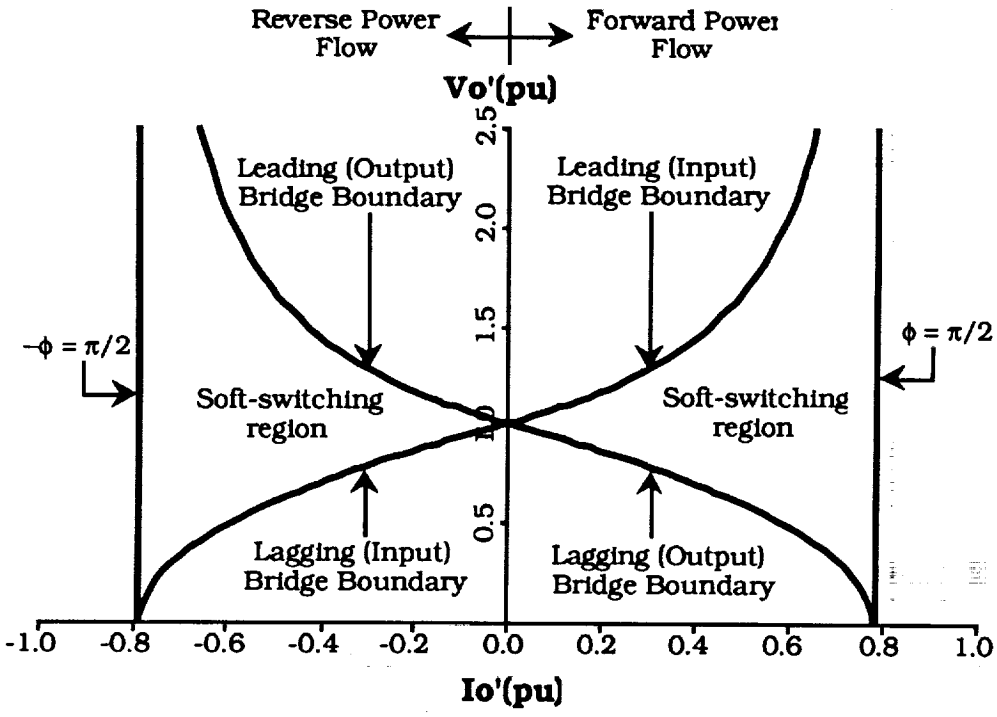


Fig. 3.3.7 Output Voltage vs Output Current, showing soft switching boundaries and regions in the two quadrants of power flow. (Topology B)

instance, the phase-shifting operation can be performed on the two legs of the input bridge (as in Topology A) and the output bridge can then be phase staggered from the input bridge in the usual manner. Or, the phase-shifting operation can be performed on both the bridges independently, and yet have them phase-staggered from each other by a controlled angle. It can be seen that each of these control schemes have more than one degree of freedom, and hence make the analysis relatively more complex. Moreover, they would probably provide access to different regions of operation, under soft switching, on the V_O' - I'_O plane.

To reduce the harmonic content of the input and output bridge currents, and hence the filter sizes this topology can be extended to a 3-phase version, with the possible concomitant benefit of reduced VA stresses on the switching devices. The following section investigates this new extension of Topology B.

3.4 Three-Phase Dual Active Bridge DC/DC Converter

Fig. 3.4.1(a) shows the circuit schematic of this circuit referred to as Topology C. It is simply a three-phase extension of Topology B. The two three-phase active bridges operate in a six-step mode at a fixed frequency. The controlled phase-shift, ϕ, between the bridges governs the amount of power flow. The high frequency ac link transformer is Y-Y connected and is three-phase symmetric with the leakage inductances used as the main energy transfer elements.

Appendix A shows a possible construction of such a transformer and also presents a simplified inductance model leading to the primary-referred equivalent circuit shown in Fig. 3.4.1(b). L is the total leakage inductance per phase referred to the primary side. Two distinct regions of operation over the range of the control parameter, ϕ, are identified.

i) Region I : $0 \leq \phi < \frac{\pi}{3}$

ii) Region II : $\frac{\pi}{3} \leq \phi < \frac{\pi}{2}$

Further, in each region <u>six</u> modes of operation exist. Fig. 3.4.2a, b show typical operating waveforms for Regions I and II, respectively. In each mode, the inductor current of Phase-a, i_{ap}, as a function of $\theta = \omega t$, where ω is the switching frequency, is given by,

$$i_{ap}(\theta) = \frac{[v_{ap}(\theta) - v_{as}'(\theta)]}{\omega L}(\theta - \theta_i) + i_{ap}(\theta_i) \qquad \theta_i \leq \theta < \theta_f$$

...(3.4.1)

where, θ_i and θ_f are the start and end of each mode respectively, v_{ap} is the Phase-a primary to neutral voltage, v_{as}' is the Phase-a secondary voltage referred to the primary side and $i_{ap}(\theta_i)$ is the initial current of each mode. The entire analysis presented below is for net power transfer from the input bridge to the output bridge.

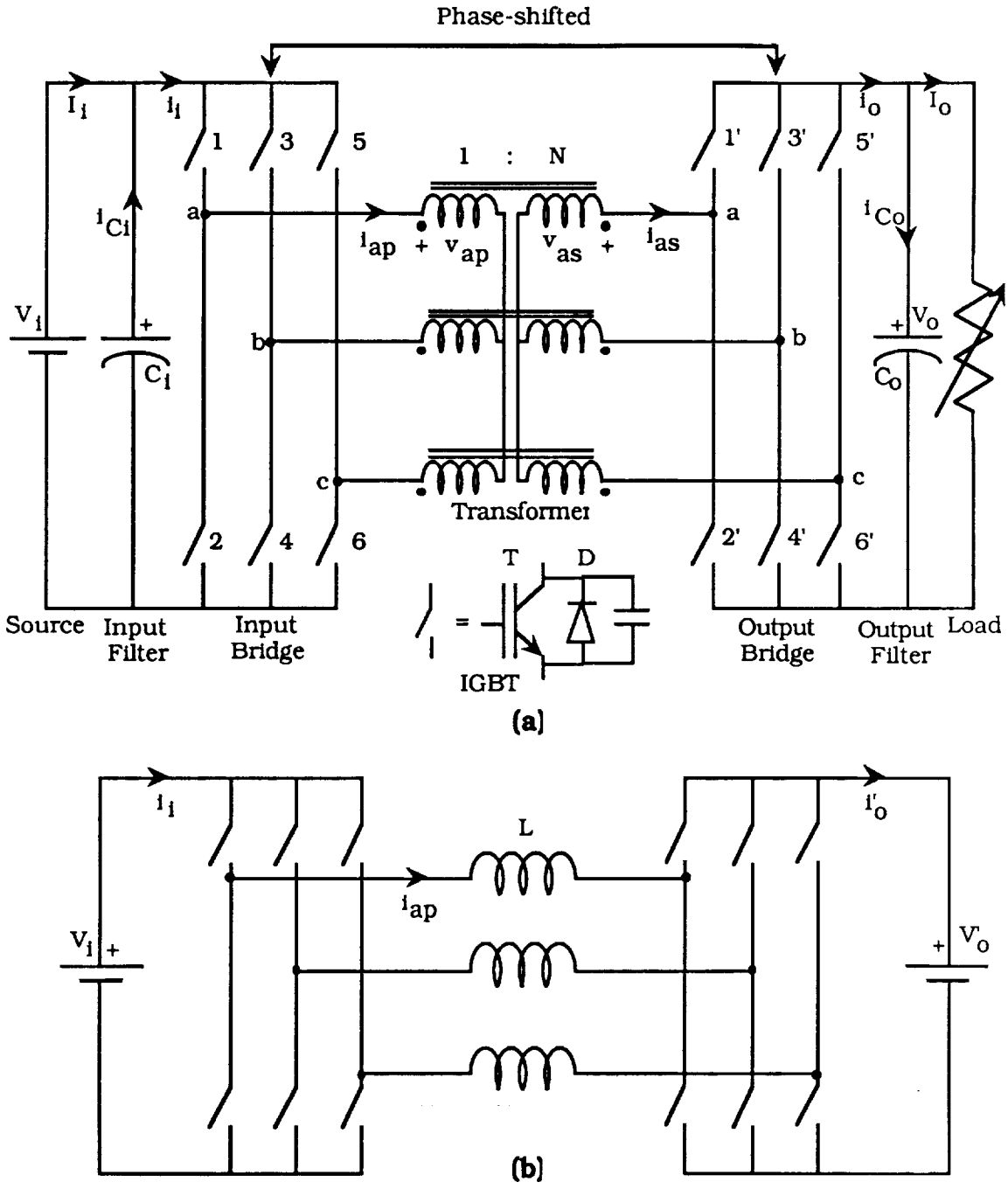


Fig. 3.4.1 (a) Circuit schematic of Three-Phase Dual Active Bridge DC/DC Converter (Topology C). (b) Primary referred equivalent circuit.

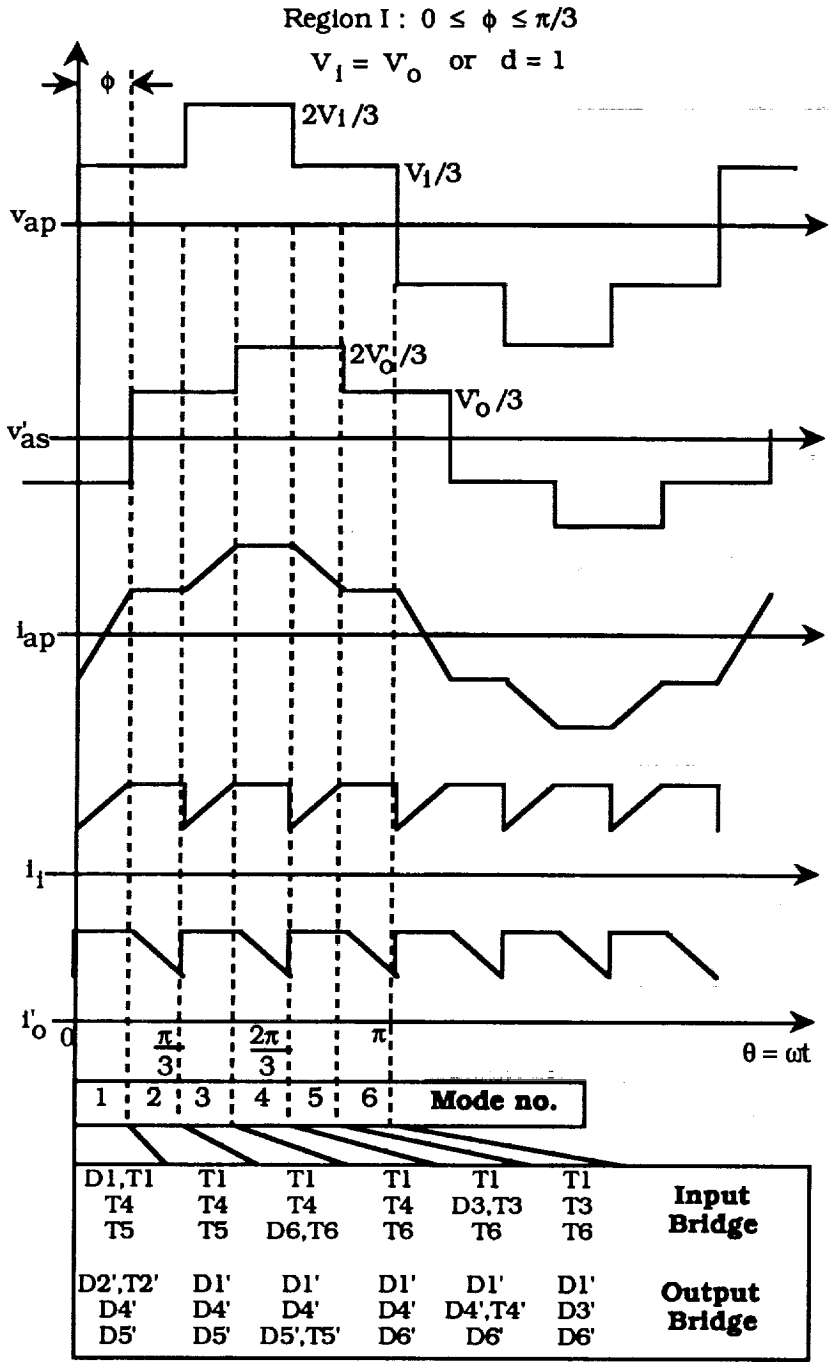


Fig. 3.4.2a Ideal operating waveforms for Topology C in Region I.

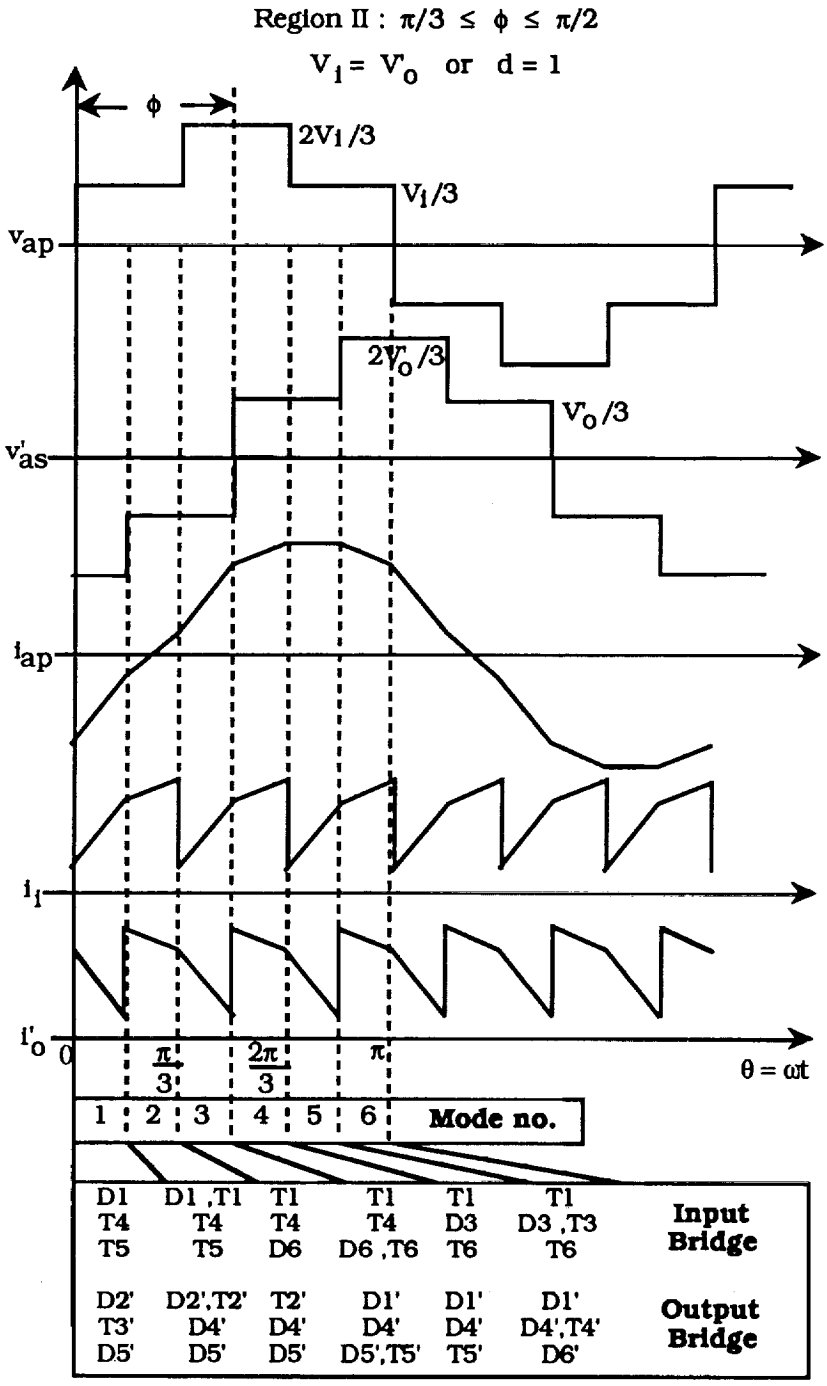


Fig. 3.4.2b Ideal operating waveforms for Topology C in Region II.

This further implies that the input bridge leads the output bridge (or, for $\phi \geq 0$). Analysis for reverse power flow ($\phi \leq 0$) is identical.

Region I (Fig. 3.4.2a) :

Mode 1 : $0 \leq \theta < \phi$; $\quad v_{ap}(\theta) = V_i/3$; $\quad v_{as}'(\theta) = -V_o'/3$

$$i_{ap}(\theta) = \frac{V_i + V_o'}{3\omega L}(\theta) + i_{ap}(0) \qquad \ldots(3.4.2a)$$

Mode 2 : $\phi \leq \theta < \pi/3$; $\quad v_{ap}(\theta) = V_i/3$; $\quad v_{as}'(\theta) = V_o'/3$

$$i_{ap}(\theta) = \frac{V_i - V_o'}{3\omega L}(\theta - \phi) + i_{ap}(\phi) \qquad \ldots(3.4.3a)$$

Mode 3 : $\pi/3 \leq \theta < (\phi + \pi/3)$; $\quad v_{ap}(\theta) = 2V_i/3$; $\quad v_{as}'(\theta) = V_o'/3$

$$i_{ap}(\theta) = \frac{2V_i - V_o'}{3\omega L}(\theta - \frac{\pi}{3}) + i_{ap}(\frac{\pi}{3}) \qquad \ldots(3.4.4a)$$

Mode 4 : $(\phi + \pi/3) \leq \theta < 2\pi/3$; $\quad v_{ap}(\theta) = 2V_i/3$; $\quad v_{as}'(\theta) = 2V_o'/3$

$$i_{ap}(\theta) = \frac{2(V_i - V_o')}{3\omega L}(\theta - \phi - \frac{\pi}{3}) + i_{ap}(\phi + \frac{\pi}{3}) \qquad \ldots(3.4.5a)$$

Mode 5 : $2\pi/3 \leq \theta < (\phi + 2\pi/3)$; $\quad v_{ap}(\theta) = V_i/3$; $\quad v_{as}'(\theta) = 2V_o'/3$

$$i_{ap}(\theta) = \frac{V_i - 2V_o'}{3\omega L}(\theta - \frac{2\pi}{3}) + i_{ap}(\frac{2\pi}{3}) \qquad \ldots(3.4.6a)$$

Mode 6 : $(\phi + 2\pi/3) \le \theta < \pi$; $v_{ap}(\theta) = V_i/3$; $v_{as}'(\theta) = V_o'/3$

$$i_{ap}(\theta) = \frac{V_i - V_o'}{3\omega L}\left(\theta - \phi - \frac{2\pi}{3}\right) + i_{ap}\left(\phi + \frac{2\pi}{3}\right) \qquad ...(3.4.7a)$$

Again, from half-cycle symmetry conditions and using eqns. (3.4.2a) - (3.4.7a), $i_{ap}(0)$ and hence, the complete current waveform can be obtained. The expressions for the current (phase 'a) at the six unique switching instants are presented in Appendix B. To determine the soft-switching constraints the current at the times of interest, $\theta = 0$ and ϕ, are repeated below,

$$i_{ap}(0) = \frac{V_i}{3\omega L}\left[\frac{2\pi d}{3} - d\phi - \frac{2\pi}{3}\right] \qquad ...(3.4.8a)$$

$$i_{ap}(\phi) = \frac{V_i}{3\omega L}\left[\frac{2\pi d}{3} + \phi - \frac{2\pi}{3}\right] \qquad ...(3.4.9a)$$

where, $d = \frac{V_o'}{V_i}$

Region II (Fig. 3.4.2b) :

Mode 1 : $0 \le \theta < (\phi - \pi/3)$; $v_{ap}(\theta) = V_i/3$; $v_{as}'(\theta) = -2V_o'/3$

$$i_{ap}(\theta) = \frac{V_i + 2V_o'}{3\omega L}(\theta) + i_{ap}(0) \qquad ...(3.4.2b)$$

Mode 2 : $(\phi - \pi/3) \le \theta < \pi/3$; $v_{ap}(\theta) = V_i/3$; $v_{as}'(\theta) = -V_o'/3$

$$i_{ap}(\theta) = \frac{V_i + V_o'}{3\omega L}(\theta - \phi + \frac{\pi}{3}) + i_{ap}(\phi - \frac{\pi}{3}) \qquad ...(3.4.3b)$$

Mode 3 : $\pi/3 \le \theta < \phi$; $v_{ap}(\theta) = 2V_i/3$; $v_{as}'(\theta) = -V_o'/3$

$$i_{ap}(\theta) = \frac{2V_i + V_o'}{3\omega L}(\theta - \frac{\pi}{3}) + i_{ap}(\frac{\pi}{3}) \qquad ...(3.4.4b)$$

Mode 4 : $\phi \le \theta < 2\pi/3$; $v_{ap}(\theta) = 2V_i/3$; $v_{as}'(\theta) = V_o'/3$

$$i_{ap}(\theta) = \frac{2V_i - V_o'}{3\omega L}(\theta - \phi) + i_{ap}(\phi) \qquad ...(3.4.5b)$$

Mode 5 : $2\pi/3 \le \theta < (\phi + \pi/3)$; $v_{ap}(\theta) = V_i/3$; $v_{as}'(\theta) = V_o'/3$

$$i_{ap}(\theta) = \frac{V_i - V_o'}{3\omega L}(\theta - \frac{2\pi}{3}) + i_{ap}(\frac{2\pi}{3}) \qquad ...(3.4.6b)$$

Mode 6 : $(\phi + \pi/3) \le \theta < \pi$; $v_{ap}(\theta) = V_i/3$; $v_{as}'(\theta) = 2V_o'/3$

$$i_{ap}(\theta) = \frac{V_i - 2V_o'}{3\omega L}(\theta - \phi - \frac{\pi}{3}) + i_{ap}(\phi + \frac{\pi}{3}) \qquad ...(3.4.7b)$$

From symmetry conditions, and eqns. (3.4.2b) - (3.4.7b), (note, Appendix B gives the expressions for the phase 'a' current at the six unique switching instants),

$$i_{ap}(0) = \frac{V_i}{3\omega L}\left[\pi d - 2d\phi - \frac{2\pi}{3}\right] \qquad ...(3.4.8b)$$

$$i_{ap}(\phi) = \frac{V_i}{3\omega L}\left[\frac{2\pi d}{3} + 2\phi - \pi\right] \qquad \ldots(3.4.9b)$$

Imposing the soft-switching constraints,

For Input bridge $\quad i_{ap}(0) \leq 0$

Over Region I ($0 \leq \phi < \frac{\pi}{3}$), from eqn. (3.4.8a),

$$d \leq \frac{1}{1 - \frac{3\phi}{2\pi}} \qquad \ldots(3.4.10a)$$

Over Region II ($\frac{\pi}{3} \leq \phi < \frac{\pi}{2}$), from eqn. (3.4.8b),

$$d \leq \frac{1}{\frac{3}{2} - \frac{3\phi}{\pi}} \qquad \ldots(3.4.10b)$$

For Output bridge $\quad i_{ap}(\phi) \geq 0$

Over Region I ($0 \leq \phi < \frac{\pi}{3}$), from eqn. (3.4.9a),

$$d \geq 1 - \frac{3\phi}{2\pi} \qquad \ldots(3.4.11a)$$

Over Region II ($\frac{\pi}{3} \leq \phi < \frac{\pi}{2}$), from eqn. (3.4.9b),

$$d \geq \frac{3}{2} - \frac{3\phi}{\pi} \qquad \ldots(3.4.11b)$$

Again, violation of any of the above constraints leads to natural commutation of the active devices and, hence, undesirably high switching losses due to the snubber dump action.

With a knowledge of the primary current, $i_{ap}(\theta)$, and the converter switching functions the various quantities of interest defined in the previous sections are calculated, and are given below.

Output Power :

For Region I ($0 \leq \phi < \frac{\pi}{3}$)

$$P_o = \left[\frac{V_i^2}{\omega L}\right] d\,\phi \left[\frac{2}{3} - \frac{\phi}{2\pi}\right] \qquad \ldots(3.4.12a)$$

For Region II ($\frac{\pi}{3} \leq \phi < \frac{\pi}{2}$)

$$P_o = \left[\frac{V_i^2}{\omega L}\right] d \left[\phi - \frac{\phi^2}{\pi} - \frac{\pi}{18}\right] \qquad \ldots(3.4.12b)$$

Transformer kVA :

$$T\_kVA = \frac{3\,(v_{aprms} + v_{asrms}')\,^* i_{aprms}}{2} \qquad \ldots(3.4.13)$$

where, $v_{aprms} = \frac{\sqrt{2}\,V_i}{3}$; $v_{asrms}' = \frac{\sqrt{2}\,V_o'}{3}$

The remaining quantities of interest are given as in Section 3.2. The steady state operating characteristics of each quantity of interest, normalized to the same base as defined in the previous sections, are plotted as a function of the control variable, ϕ, with d as a parameter.

Fig. 3.4.3a shows the variation of output power as a function of ϕ, over the range 0 to π / 2, with d as a parameter. The trend is similar to that of Topology B (Fig. 3.3.3a). However, for $d < 1$, soft-switching can be obtained over a marginally higher range of ϕ, as compared to Topology B. For $d = 1$, full control over ϕ is attainable, under soft-switching. Fig. 3.4.3b shows the same for values of $d > 1$. This demonstrates boost mode of operation under soft-switching. Analysis has been carried out for operation in the first quadrant only. But, given the symmetry of the converter, it can be shown that reverse power flow characteristics similar to those for Topology B (Figs. 3.3.3a and 3.3.3b) can be realized.

Figs. 3.4.4a and 3.4.4b show the variation of transformer kVA with ϕ and output power respectively. Selecting the maximum power transfer point (0.267pu) on the output bridge constraint (which pertains to the output bridge operating as a diode bridge), the minimum transformer kVA required is 0.391pu, Fig. 3.4.4b. This gives a transformer utilization of 0.683. Now, for the same transformer kVA, the output power can be increased to 0.351pu at d = 1 (see point labelled X), by virtue of an active output bridge. Hence,

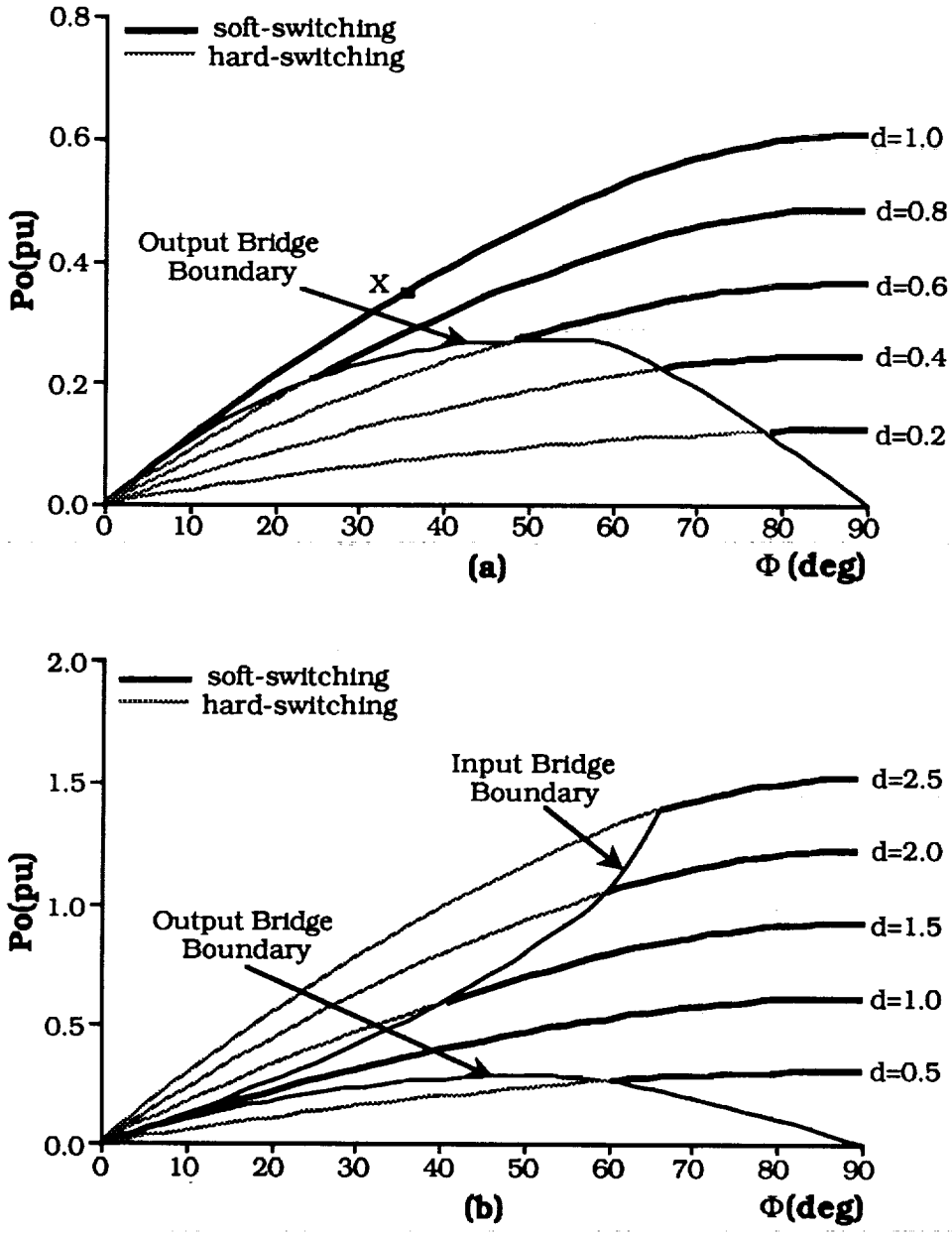


Fig. 3.4.3 (a) Output Power vs ϕ with d as a parameter, showing buck characteristics. (b) Output Power vs ϕ with d as a parameter, showing buck-boost characteristics. (Topology C)

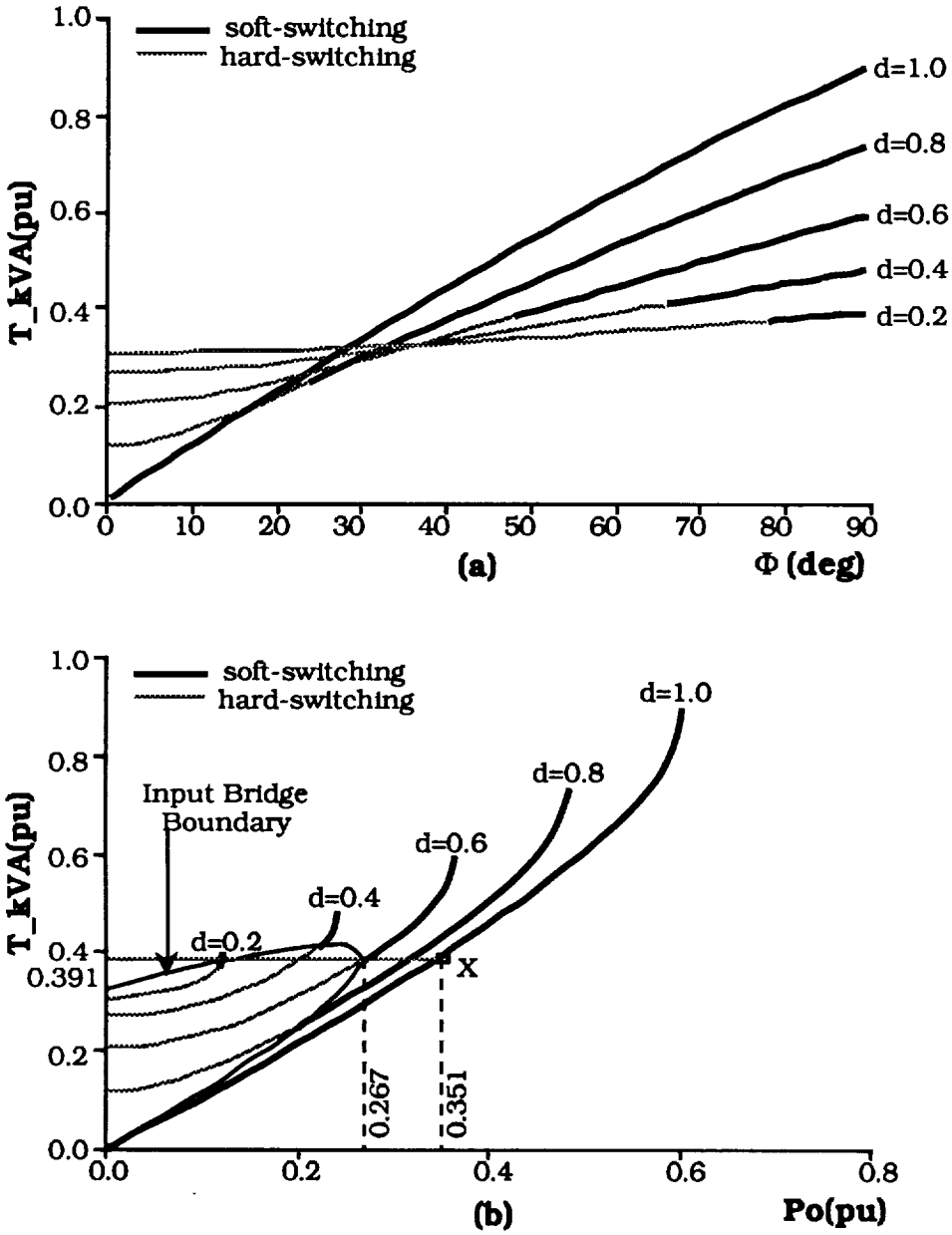


Fig. 3.4.4 (a) Transformer kVA vs ϕ with d as a parameter. (b) Transformer kVA vs P_o with d as a parameter. (Topology C)

transformer utilization has gone up to 0.898, an increase of 31%. Moreover, the transformer utilization is fairly constant over a wide range of ϕ at d = 1, a very desirable feature.

The variation of input and output filter capacitor kVA (or, r.m.s. ripple currents) with ϕ and output power are shown in Figs. 3.4.5a,b and 3.4.6a,b. For lower values of d, the output current ripple increases. However, as expected, under all conditions the ripple is substantially smaller than for either of the single phase topologies. This can be verified from comparing their relative kVA ratings at any given operating point. A characteristic feature of Topology C, with regard to filter capacitor r.m.s. currents (and, hence kVA ratings), should be brought to light. At ϕ = 60° and d=2.0 (see Fig. 3.4.5a) the input filter capacitor r.m.s. current is *zero*, and for the same phase-shift at d=0.5 (see Fig. 3.4.6a), the output filter capacitor r.m.s. current is *zero*. To illustrate these operating points, a simulation of Topology C with the complete 3-phase transformer model was carried out. Fig. 3.4.7a, shows the transformer a-phase voltages(v_{ap}, v_{as}') and current(i_{ap}) and the bridge currents(i_i, i_o') for the case where i_i is a constant, showing no ripple components. Likewise, Fig. 3.4.7b depicts the case where i_o' is ripple-free. Clearly, given the operating range of the converter, an optimization is possible which yields the smallest *total* filter size.

Finally, Fig. 3.4.8 depicts the region of soft-switching on the V_o' - I'_o plane. Observations similar to that for Topology B can be drawn.

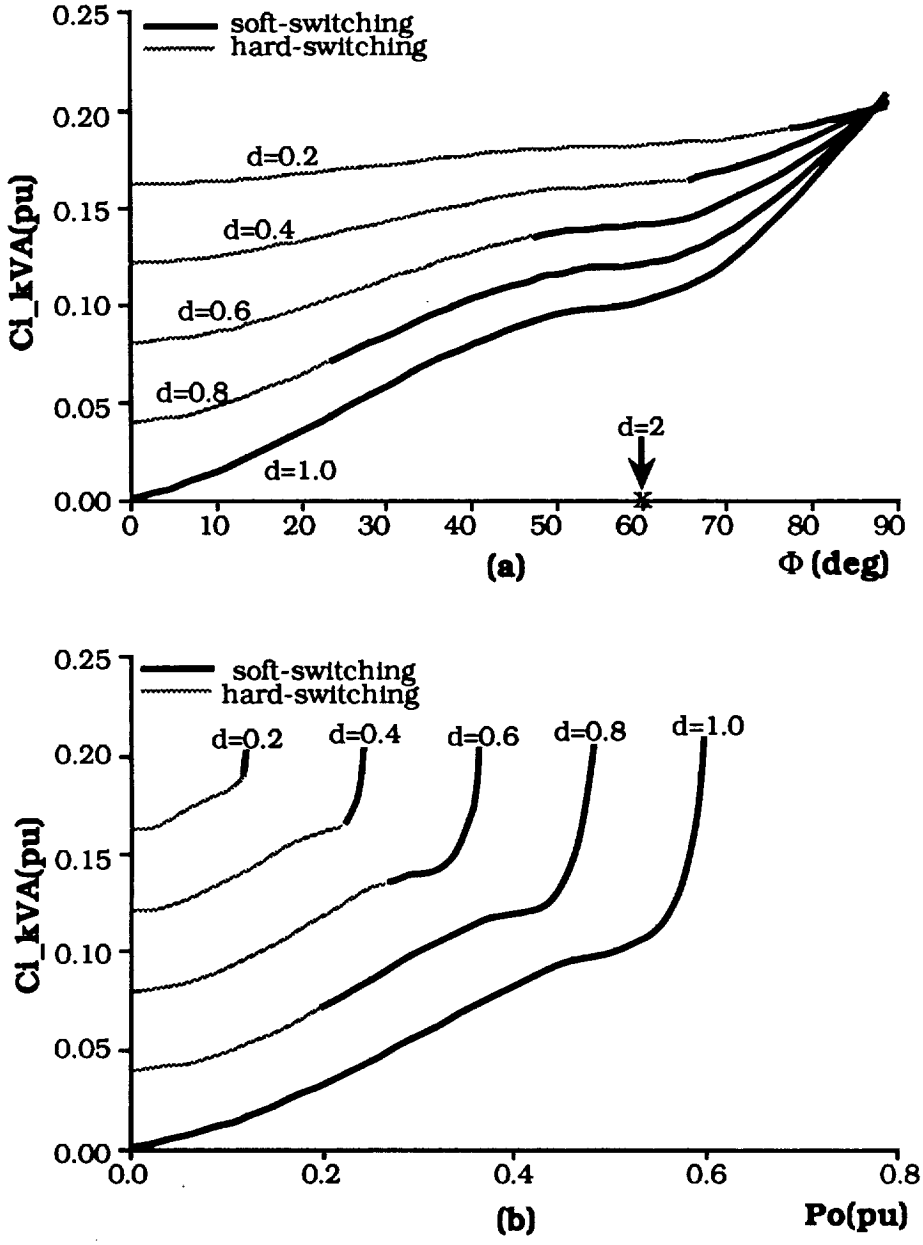


Fig. 3.4.5 (a) Input Filter Capacitor kVA vs ϕ with d as a parameter. (b) Input Filter Capacitor kVA vs P_o with d as a parameter. (Topology C)

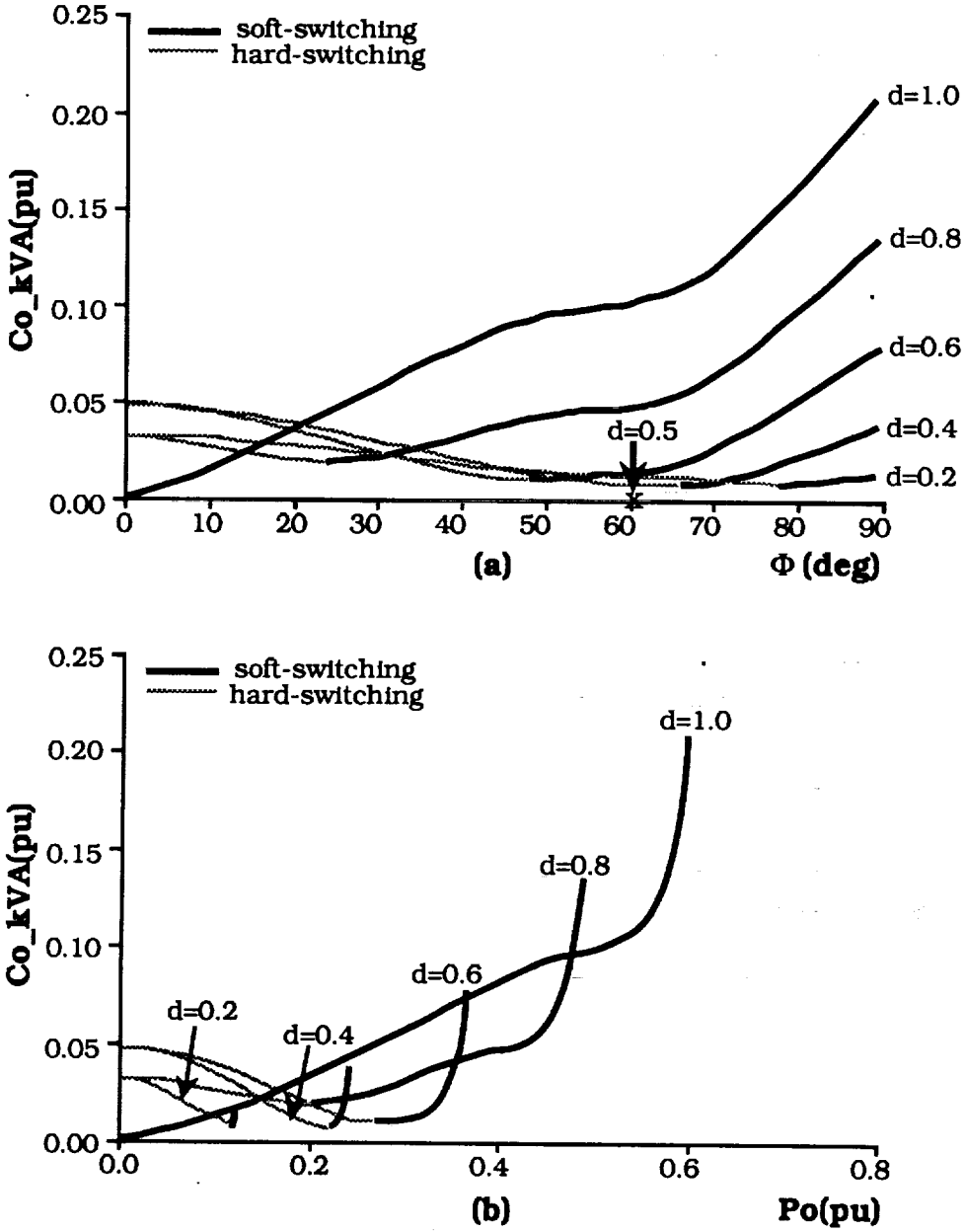


Fig. 3.4.6 (a) Output Filter Capacitor kVA vs ϕ with d as a parameter. (b) Output Filter Capacitor kVA vs P_o with d as a parameter. (Topology C)

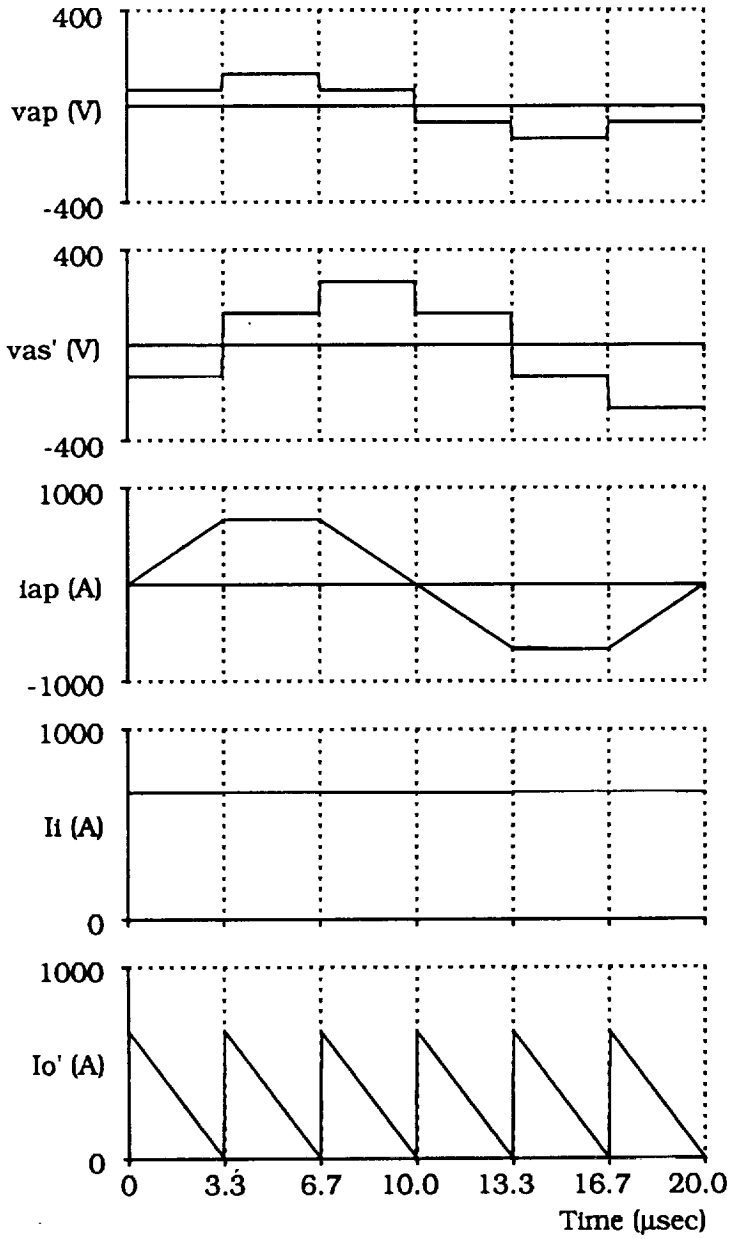


Fig. 3.4.7 (a) Simulation of Topology C, for d=2, ϕ=60°, showing the ripple-free input bridge current, i_i. Input bus voltage = 200Vdc, Output bus voltage = 400Vdc, transformer turns ratio = 1:1, Switching frequency = 50kHz.

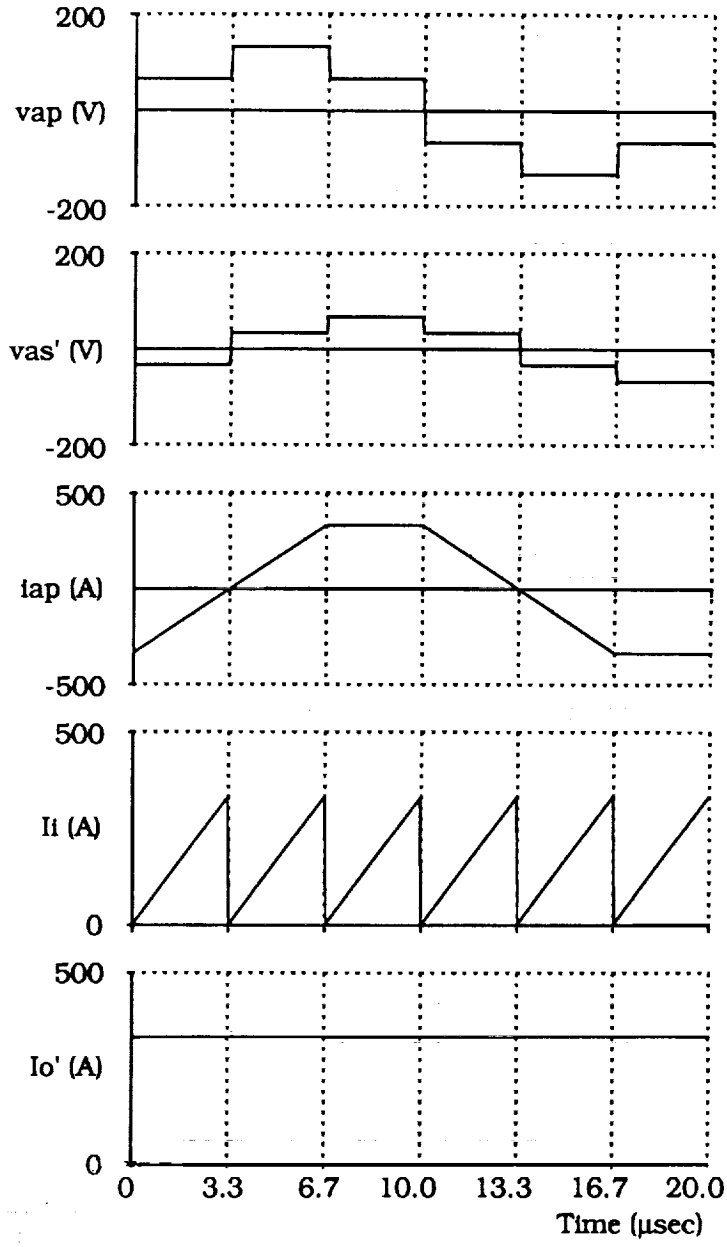


Fig. 3.4.7 (b) Simulation of Topology C, for d=0.5, ϕ=60°, showing the ripple-free output bridge current, i_o'. Input bus voltage = 200Vdc, Output bus voltage = 400Vdc, transformer turns ratio = 1:1, Switching frequency = 50kHz.

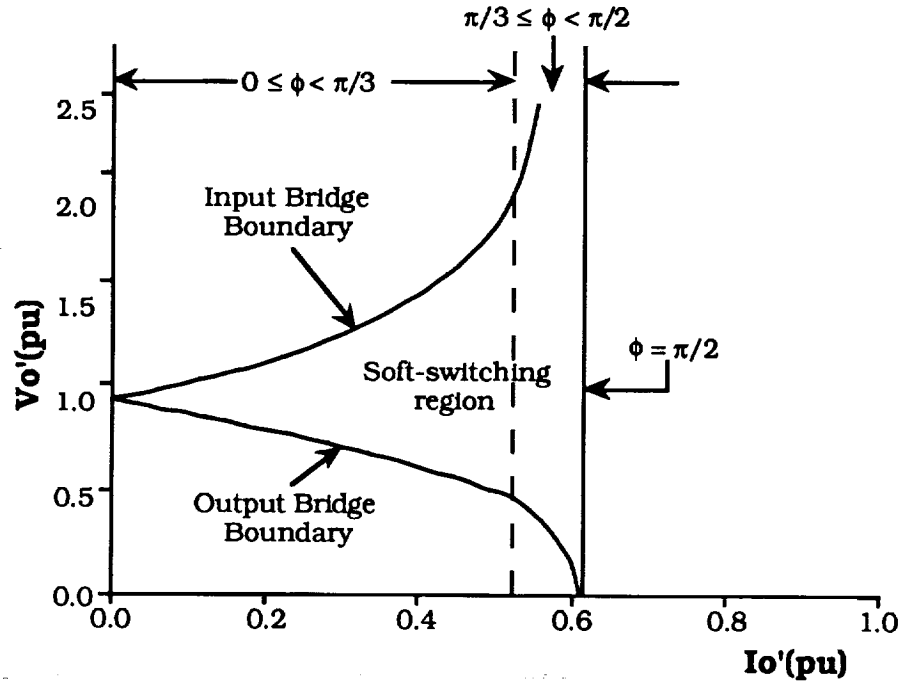


Fig. 3.4.8 Output Voltage vs Output Current, showing the soft switching region and its boundaries. (Topology C)

One might be tempted to further extend the three-phase version to a general n-phase system. This would certainly be advantageous as far as the filter size is concerned. However, the cost and design of an n-phase transformer and the increasing number of active devices with their control and drivers would soon offset the decrease in cost of the filters. Additionally, the analysis would become extremely tedious with the multiple regions and modes of operation.

In the following section, an elegantly simple model is presented for Topologies B and C. The model is based on the fundamental component and improves understanding of the operation of these circuits.

3.5 Fundamental Model for Proposed Topologies B and C

Conceptually, each of these circuits can be viewed as an inductor (the transformer leakage inductance) driven at either end by a controlled square-wave voltage source. The voltage sources are phase-shifted from each other by a controlled angle, ϕ. To simplify the analysis, the square-wave voltage sources are replaced by their fundamental components. Fig. 3.5.1a shows the fundamental model. Note, this model can also be treated as a per phase model for Topology C. The model is identified to the familiar synchronous machine equivalent circuit and may be expected to demonstrate similar properties. The inductance, L, is analogous to the series

inductance of the machine. The input ($\mathbf{V_{fi}}$) and output ($\mathbf{V_{fo}'}$) voltage sources can be viewed as the internal e.m.f. and terminal voltage, respectively. The angle, ϕ, is commonly referred to as the torque angle. Since, all circuit quantities are sinusoidal at a single frequency (the switching frequency), a phasor analysis can be carried out. The steady state current phasor, $\mathbf{I_p}$, through the inductor, is given as,

$$I_p = \frac{V_{fi} - V_{fo}'}{X_L} \qquad \ldots(3.5.1)$$

where, $\mathbf{V_{fi}} = V_{fi}\langle 0\rangle$; $\mathbf{V_{fo}'} = V_{fo}'\langle -\phi\rangle$

$\mathbf{X_L} = j\omega L$; ω = switching frequency

Note, for a square-wave input voltage of peak amplitude V_i, the r.m.s. fundamental component, V_{fi} is given as,

$$V_{fi} = \frac{2\sqrt{2}V_i}{\pi}$$

Similarly, for the output,

$$V_{fo} = \frac{2\sqrt{2}V_o}{\pi}$$

Hence, the output power is given as,

$$P_o = \text{Real part of} \left[\mathbf{V_{fo}'}\ \mathbf{I_p^*}\right]$$

$$= \frac{V_{fi}^2}{\omega L} d \sin(\phi) \qquad \ldots(3.5.2)$$

where, $d = \frac{V_{fo}'}{V_{fi}}$

Eqn. (3.5.2) is identical to that for a synchronous machine. Fig. 3.5.1b shows a plot of the fundamental output power(normalized to the power base defined in Section 3.2) for d = 1. The actual output power for Topology B, for d = 1, is also shown on the same figure. The good correlation, justifies the validity of the fundamental model.

To appreciate the relationship between ϕ and d for soft-switching conditions, phasor diagrams based on the fundamental model can be very helpful. Again, as a reminder the soft-switching constraints dictate that the inductor current $\mathbf{I_p}$ lag the input voltage, $\mathbf{V_{fi}}$, and lead the output voltage, $\mathbf{V_{fo}'}$. For instance, Fig. 3.5.2a shows the phasor diagram for d = 1. As ϕ is varied over the range 0 to $\pi/2$, the current phasor, $\mathbf{I_p}$ always remains between the phasors $\mathbf{V_{fi}}$ and $\mathbf{V_{fo}'}$, thus satisfying the above soft-switching constraints for this entire range of ϕ. This conforms to our actual model. Fig. 3.5.2b shows another phasor diagram, where d < 1. As seen, ϕ must be greater than a certain minimum to achieve soft-switching on the output bridge. The input bridge constraint is always satisfied.

A fundamental model for the dual active bridge topologies has been presented. The model shows good correlation in the actual model. Hence, the simple analysis for the fundamental model can be used in making some first-pass predictions about the operation of

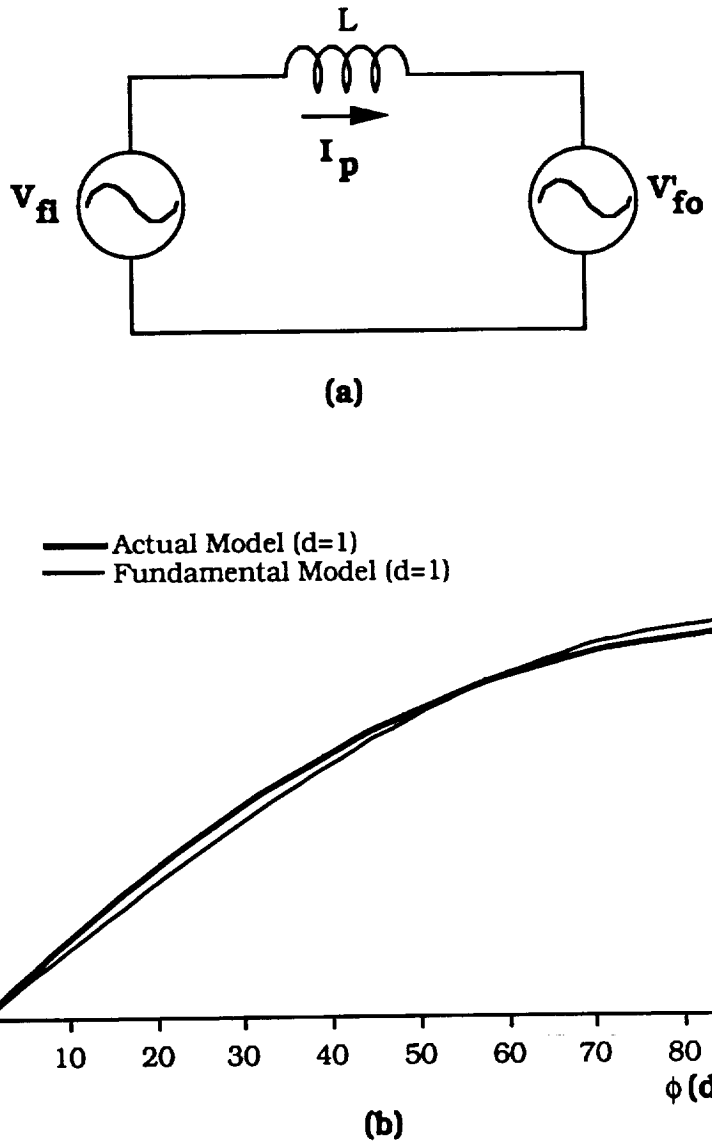


Fig. 3.5.1 (a) Fundamental model of Dual Active Bridge DC/DC Converter. (Per phase model for Topology C). (b) Output power vs ϕ for Actual and Fundamental models at d = 1.

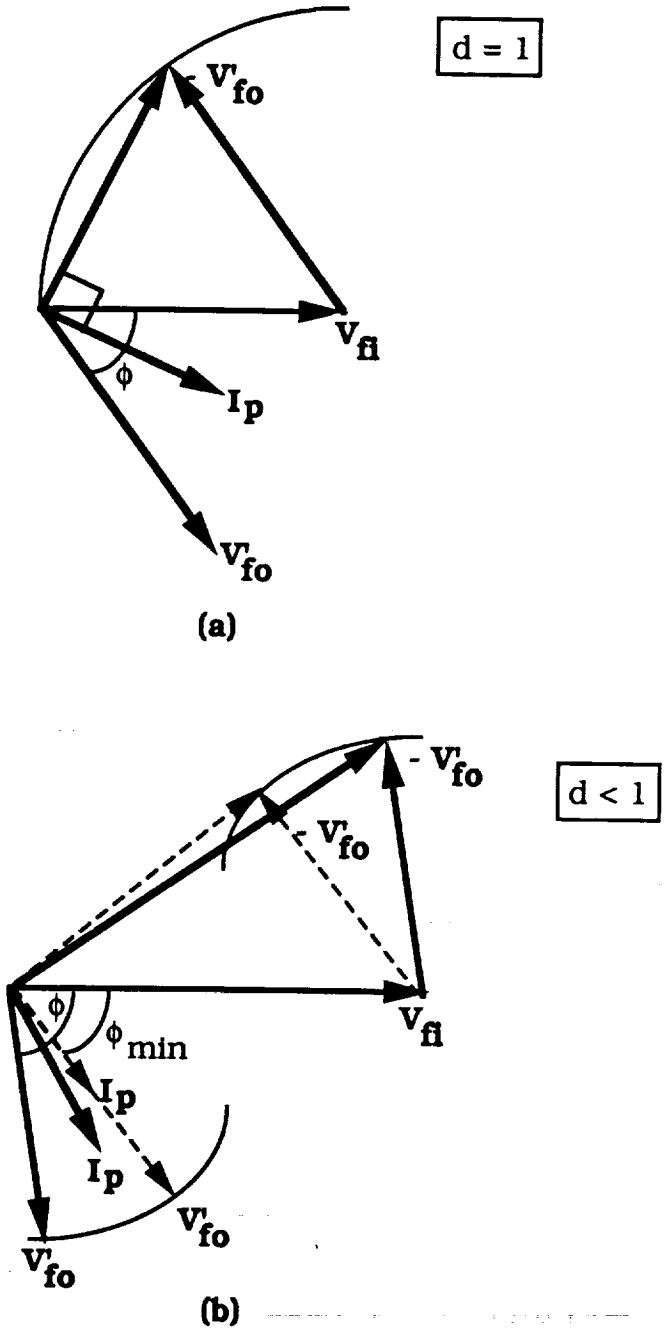


Fig. 3.5.2 Phasor diagram for the fundamental model for (a) d=1 (b) d < 1. These diagrams show the relative positions of the voltage and current phasors that must be maintained for soft-switching.

the circuit. Moreover, the phasor diagrams are a convenient tool for understanding the soft-switching constraints for the two bridges.

3.6 Small Signal Behaviour of Topology B

The following is a study of the small-signal low-frequency response [24] of the dual active bridge converter. The purpose of this analysis is to demonstrate the simple but robust first-order characteristics of the converter, manifesting from the current-controlled output. The control-to-output and input-to-output small signal transfer functions are derived from the steady-state output current. The average output current about a steady-state operating point, ϕ, derived in Section 3.3, is rewritten as

$$I_o = K\psi\,(2 - \psi) = K\,(2\psi - \psi^2) \qquad \ldots(3.6.1)$$

where,

$$K = \frac{V_i}{8f\,LN}$$

N = secondary/primary turns ratio

$$\psi = \frac{\phi}{\pi/2}\ (\text{normalized } \phi)$$

Control (ψ) to Output (V_o) transfer function :

Keeping input voltage, V_i and frequency, f, constant let $\Delta\psi$ be a small disturbance around the operating point, ψ, which causes a small disturbance of ΔI_o about I_o and, hence, a disturbance ΔV_o about V_o . Therefore, from eqn. (3.6.1)

$$I_o + \Delta I_o = K[\psi + \Delta\psi][2 - \psi - \Delta\psi]$$

or,

$$\Delta I_o = 2K[1 - \psi]\Delta\psi \qquad \ldots(3.6.2)$$

For the small-signal low-frequency (<< switching frequency) behaviour the output load circuit of the dual active bridge converter can be simply modelled as shown below in Fig. 3.6.1.

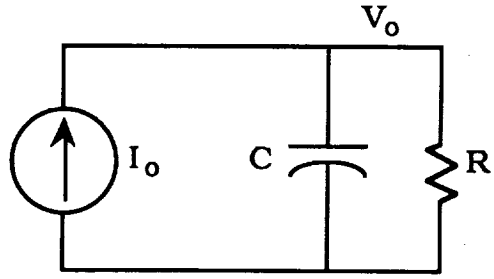


Fig. 3.6.1 Equivalent output load circuit for small-signal, low-frequency behaviour.

Hence, the small-signal perturbation of the output voltage can be written as,

$$\Delta V_o(s) = \Delta I_o(s)\ \frac{R}{1+sCR} \qquad \ldots(3.6.3)$$

Substituting eqn. (3.6.2) into eqn. (3.6.3)

$$\Delta V_o(s) = 2K[1 - \psi]\Delta\psi(s)\ \frac{R}{1+sCR}$$

or,

$$\frac{\Delta V_o(s)}{\Delta\psi(s)} = \frac{2K[1 - \psi]R}{1 + sCR} \qquad \ldots(3.6.4)$$

This is the required control-to-output transfer function demonstrating the first-order characteristic of the dual bridge converter, determined by the output capacitor and load resistance.

Input (V_i) to Output (V_o) transfer function :

Keeping control, ψ, and frequency, f, constant, let ΔV_i be a small disturbance around the operating point, V_i which causes a small disturbance of ΔI_o about I_o and, hence, a disturbance ΔV_o about V_o . Therefore, from eqn. (3.6.1),

$$I_o + \Delta I_o = \frac{V_i + \Delta V_i}{16 f LN} (2\psi - \psi^2) \qquad \ldots(3.6.5)$$

or,

$$\frac{\Delta I_o(s)}{\Delta V_i(s)} = K_1 \qquad \ldots(3.6.6)$$

where,

$$K_1 = \frac{2\psi - \psi^2}{8 f LN} = \text{constant}$$

From eqns. (3.6.3) and (3.6.6)

$$\frac{\Delta V_o}{\Delta V_i}(s) = \frac{K_1 R}{1 + sCR} \qquad \ldots(3.6.7)$$

The small-signal input-to-output gain of the converter is also characterized by a first-order roll-off. The two transfer functions, thus, demonstrate that the system will operate stably with a simple proportional controller in a closed loop configuration.

3.7 Summary

The main goal of this chapter has been to present the principle of operation along with a detailed steady state analysis for each of the three proposed topologies. The various operating characteristics including power transfer, transformer and filter kVAs, derived from this analysis, are shown, with their soft-switching and hard-switching regions. A fundamental model for the dual active bridge dc/dc converters is also presented, and is seen to give good insights into the operation of the converter through the aid of phasor diagrams. Finally, the small-signal response of Topology B indicates that the system has characteristics of a simple first-order RC-filter. The choice of the optimum topology based on the requirements of high power density, high reliability, and ease of control is addressed in the chapter on selection of converter topology.

CHAPTER 4

ANALYSIS OF DEVICE LOSSES IN THE PROPOSED TOPOLOGIES

4.1 Introduction

With the operational steady-state characteristics and relative control regions of the proposed topologies identified, it is appropriate now to address the performance of the converters from an efficiency stand-point. Converter losses can be broadly classified as active and passive component losses. With proper design and selection the passive component losses (capacitor ESR, transformer core and copper losses) can be substantially reduced. However, device losses, largely governed by their switching speeds and on-state voltages, typically are the most dominant losses in the converter. The dependence of the switching and conduction losses of the converter devices on the load and control parameters, for the three proposed topologies are thus analyzed here.

The component electrical stresses, from the previous chapter, complemented with the device losses, presented here, should form a sound basis for selecting the optimum topology for the application of interest.

4.2 Device Loss Components

4.2.1 Switching Losses

Device switching losses are a strong function of switching frequency and switching methodology. As stated earlier, for high power density converters operating at high frequencies, the use of zero-voltage/zero-current switching techniques to minimize the switching losses is an attractive alternative. In the proposed topologies, all devices operate under conditions of zero-voltage switching. The turn-on of any device is initiated while its anti-parallel diode is conducting. This ensures that the device naturally takes over as the diode current reverses, and more importantly, does so under almost zero-voltage conditions. The turn-off process must always be initiated when the device is carrying a certain minimum current. The rate of rise of voltage across the device during its turn-off is governed by the snubber capacitor. Typically, such circuits are oversnubbed to ensure near zero-voltage turn-off.

The device of choice at this time, is the Insulated Gate Bipolar Transistor (IGBT). Although the MOS-Controlled Thyristor (MCT) seems to be a better alternative from a standpoint of speed and forward drop, availability of adequately rated devices is not anticipated in the near future. A simplified model for the turn-off switching waveform for the IGBT is shown in Figure 4.2.1 [25]. I_m is the current at the instant of turn-off. The model shows that the

current through the device falls almost instantaneously to a value K^*I_m, and then decays to zero over a time, t_f, sometimes referred to as the tail time. The parameter K is extracted from test turn-off waveforms, and is typically equal to 0.25 [26, 27]. With a knowledge of the turn-off behaviour, an expression for the turn-off losses is derived (by integrating the product of the device voltage and current during the turn-off transition) and is shown in eqn. (4.2.1). The current through the transformer leakage inductance is assumed constant over the duration of the switching transition.

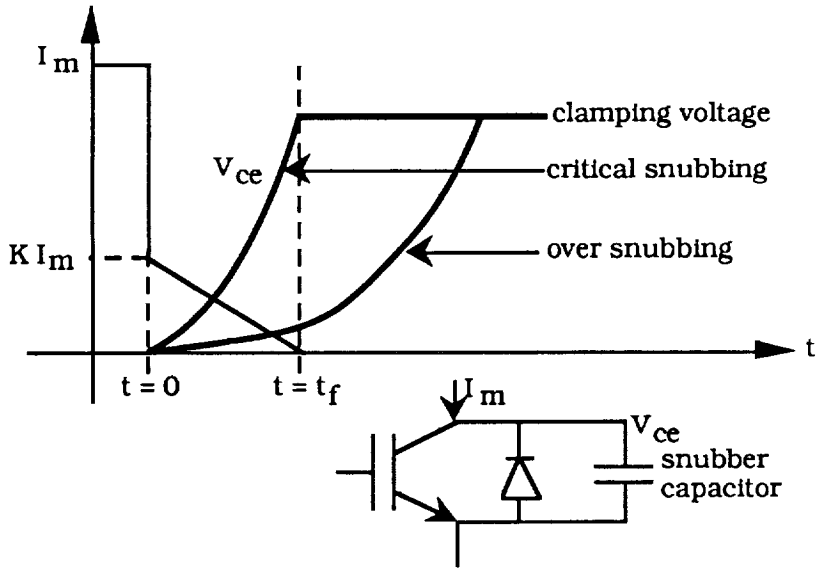


Fig. 4.2.1 Typical model for the turn-off switching behaviour of an IGBT.

$$P_{sw} / \text{device} = \frac{f I_m^2 t_f^2 (4 - 3K) K}{48 C} \qquad \ldots(4.2.1)$$

where, f is the switching frequency and C is the snubber capacitance. This expression is valid only for C greater than a critical value. The critical value of the snubber capacitance is the value for which the device voltage just reaches the bus (clamping) voltage at the end of t_f. C is designed for critical snubbing at the worst case (maximum turn-off current) over a specified operating range, thus ensuring that for normal (near rated) operation the devices are adequately oversnubbed. This worst case capacitance, $C_{s(max)}$, is given as,

$$C_{s(max)} = \frac{I_{m(max)} t_f (2 - K)}{4 V_{bus}} \qquad \ldots(4.2.2)$$

where, $I_{m(max)}$ is the maximum turn-off current seen by the device and V_{bus} is the dc bus voltage. The switching loss expressions for devices on both the bridges for each topology are given in Appendix B.

Although, in practice the diodes also incur switching losses, predominantly during reverse recovery, such losses are only a small fraction of the device switching losses by virtue of the soft turn-off mechanism. In real devices, a dominant source of loss is also due to internal package inductance, where the energy stored during turn-off is dissipated in the silicon. Diode switching losses become

appreciable for the very same reason. However, since such stray effects are secondary to the device and can be eliminated by proper packaging, their influence on the losses will be ignored in the analysis. In the experimental chapter, a separate section is devoted to the estimation of stray inductive losses and their impact on the converter efficiency.

4.2.2 Conduction Losses

The device conduction losses are computed based on the assumption that the currents flowing through the device or its anti-parallel diode are linear. This is a fair assumption for high frequency transformers, since the dominant parameter is the leakage inductance. The average current through each device and diode are first derived and multiplied by their respective on-state voltages to give the conduction loss. Since the derivation is straightforward, the detailed expressions are presented in Appendix B. With the intention of comparing the relative device losses in the three topologies the analysis is simplified under the assumptions that the turn-off transition is negligible compared to the switching period, and the ESR's (Effective Series Resistance) of the passive components are negligible.

4.3 Device Loss Characterization for the Proposed Topologies

For each topology the switching and conduction losses are computed for three different output voltages, with the control parameters swept through the entire region of soft-switching. The switching device is assumed to be the IGBT, with the device and anti-parallel diode forward drops of 3V (V_T) and 1V (V_D) respectively, and t_f = 0.5 μs. The transformer turns ratio is assumed as unity. The losses are normalized to the power base,

$$P_b = \frac{V_i^2}{2 \pi f L}$$

where, V_i is the input dc voltage, f is the switching frequency and L is the transformer leakage inductance. The normalized switching and conduction losses for the input and output bridges of each topology are presented below. The overall converter efficiency is estimated as,

$$\text{Efficiency} = \frac{P_o}{P_o + P_{loss}} \qquad \ldots(4.3.1)$$

where, P_o is the output power computed from the expressions derived in the last chapter (for each topology), and P_{loss} is the total converter device losses.

Fig. 4.3.1 shows the loss breakup as a function of β(phase-shift between the poles of the input active bridge) for Topology A, for three d's (d=0.58, β=180° is the maximum power point). Psw_i/br (Psw_o/br) is the total switching loss for the input (output) bridge devices, Pco_i/br (Pco_o/br) is the total conduction loss for the input (output) bridge devices (and diodes). It is seen that each loss component (switching and conduction) decreases with increasing d, since the peak current stresses decrease. For a given d, losses increase with β, for the same reason. Fig. 4.3.2a shows the total estimated device losses. Fig. 4.3.2b shows the variation in the estimated efficiency. The loss and efficiency figures, although not complete, are intended to give the designer a first-cut estimate of the converter performance.

Figs. 4.3.3 and 4.3.4a show the loss breakup and total device losses versus ϕ for Topology B, for three representative d's covering buck to boost modes. The increase in losses with increasing ϕ and d is a consequence of increasing peak current stresses. The switching losses tend to increase with the square of the turn-off currents. For d = 1, the switching losses on the input and output bridges are identical, since the turn-off currents are identical. The conduction losses for the output bridge are always lower than that for the input bridge because in the forward power flow mode (input phase-leading the output) the output bridge is mostly running as a rectifier, with the diodes (lower forward drop) conducting for a greater portion of

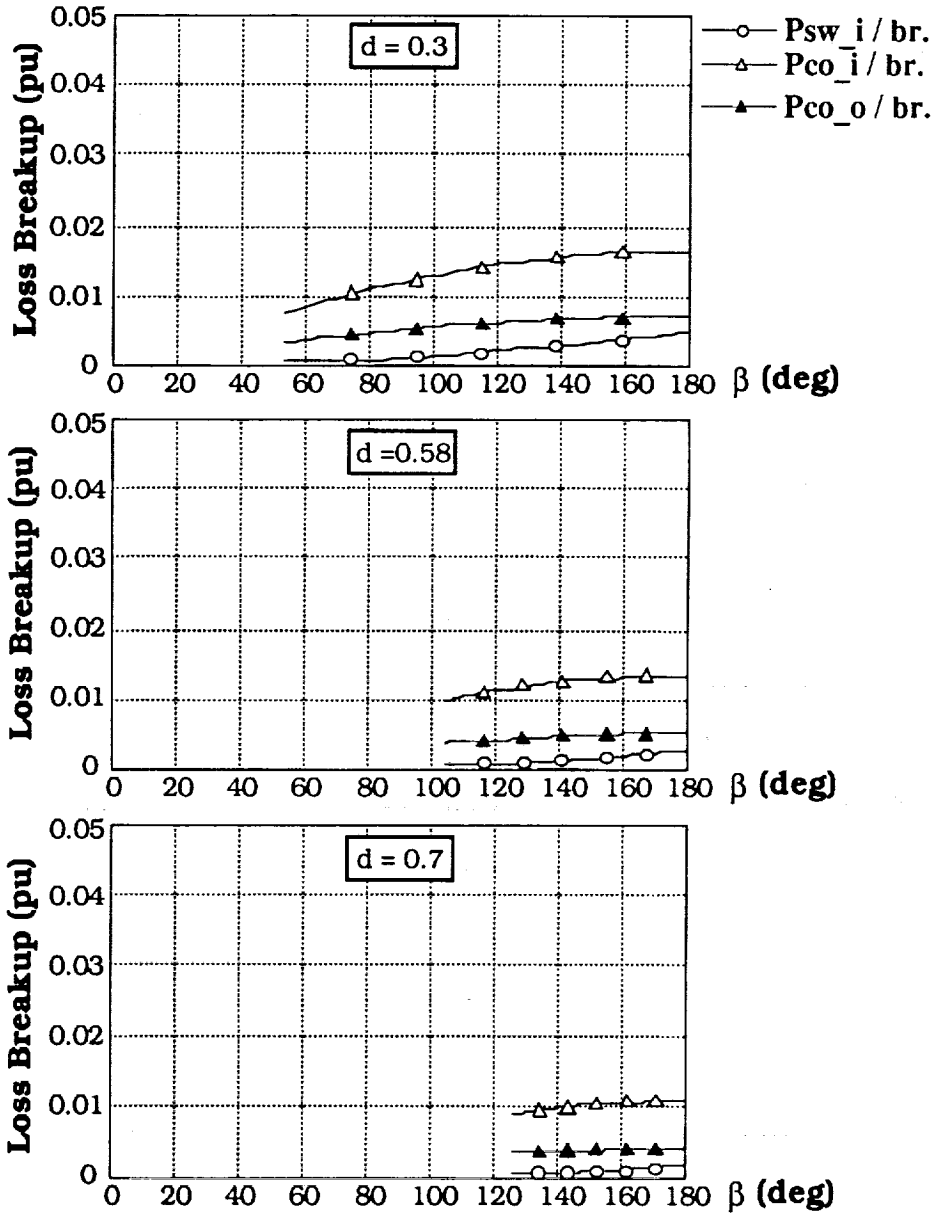


Fig. 4.3.1 Device (IGBT) Loss breakup versus β for the input and output bridges of Topology A in the soft-switching region of operation. V_i=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V.

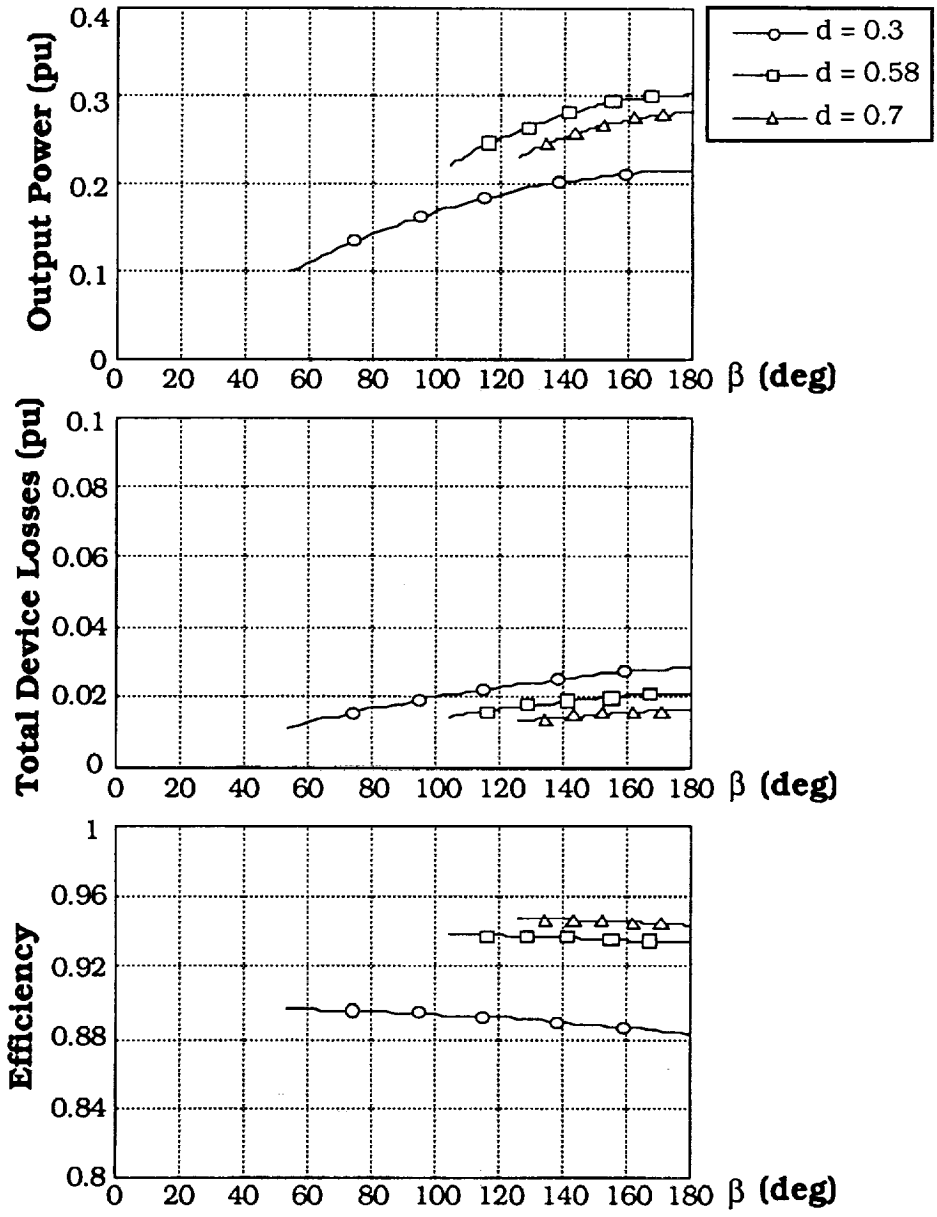


Fig. 4.3.2 Output Power, Total device losses, and projected efficiency versus β for Topology A in the soft-switching region of operation. V_i=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V.

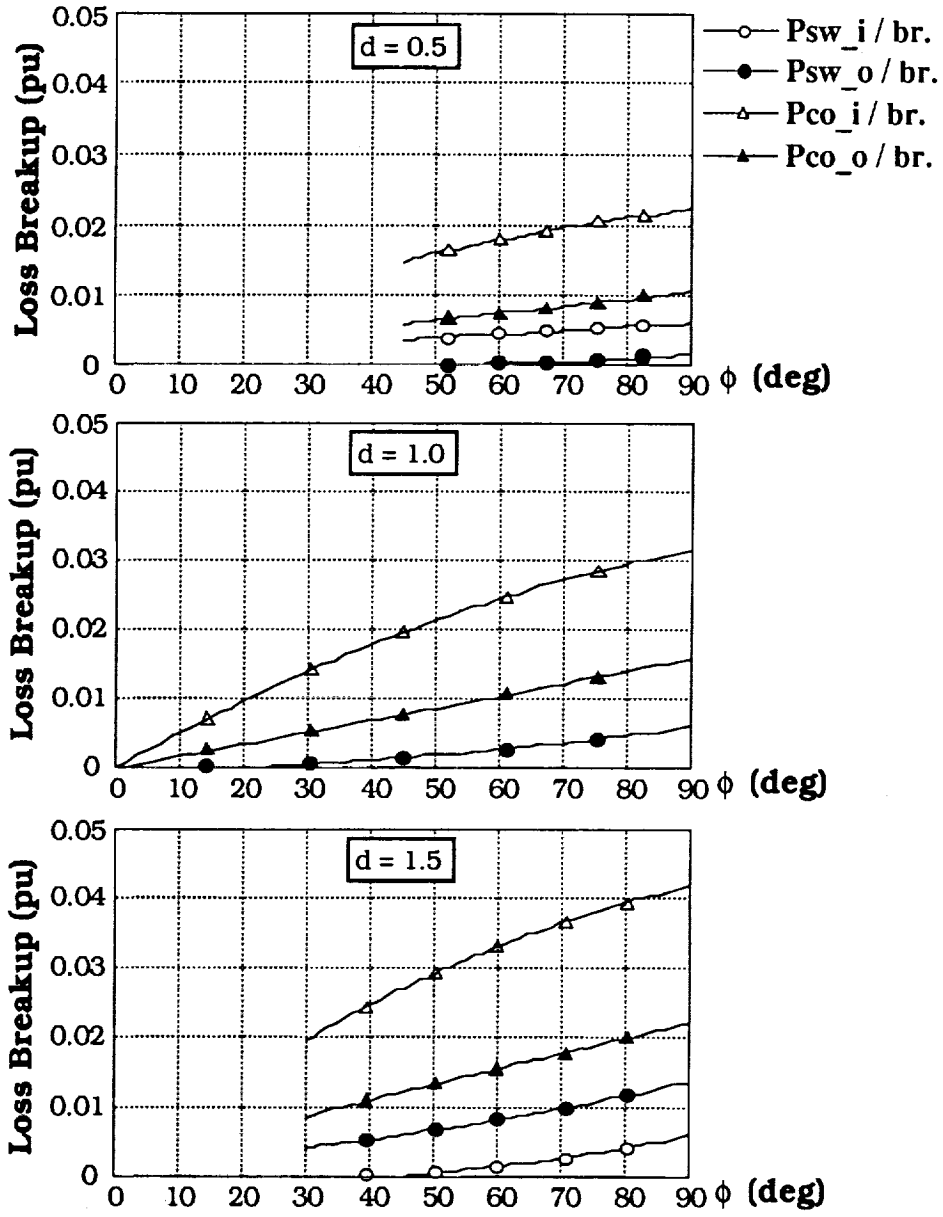


Fig. 4.3.3 Device (IGBT) Loss breakup versus ϕ, for the input and output bridges of Topology B in the soft-switching region of operation. V_i=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V.

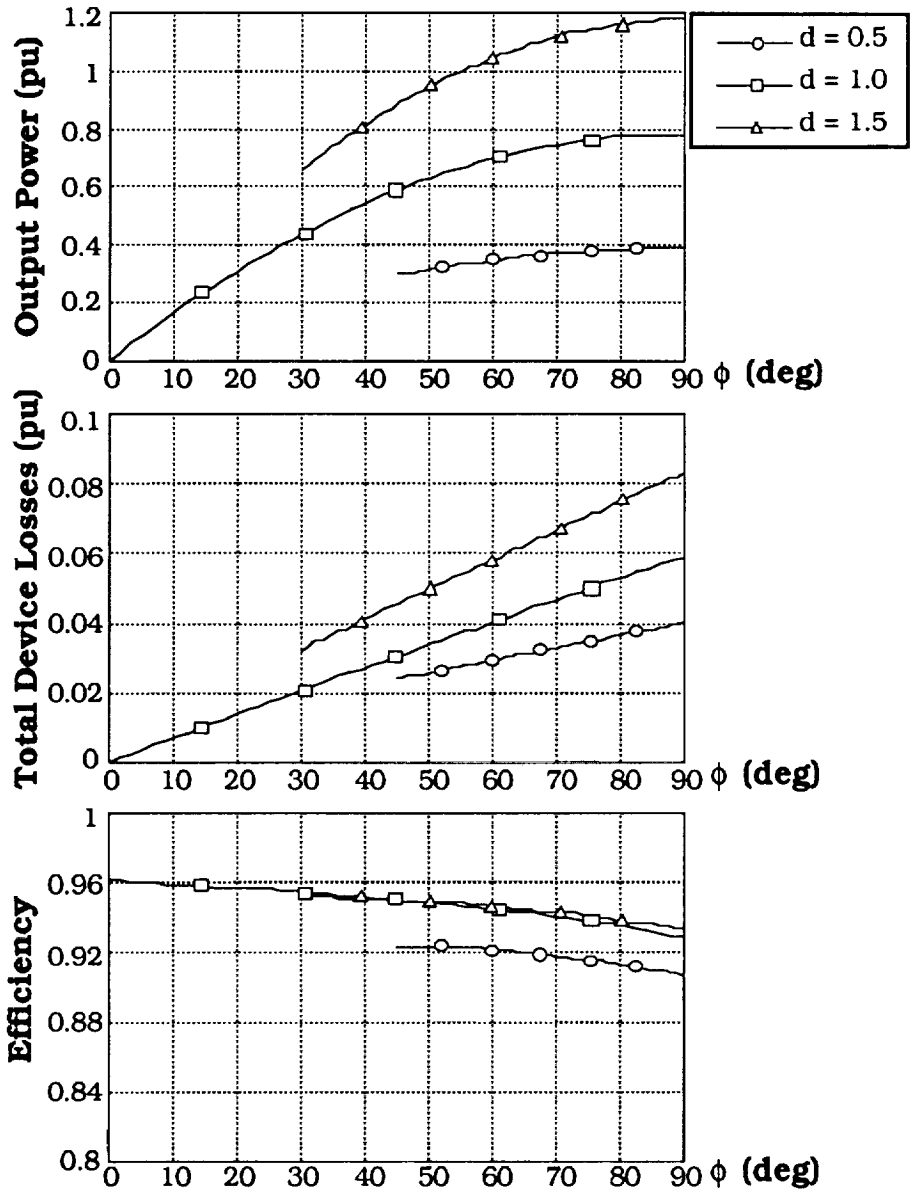


Fig. 4.3.4 Output Power, total device losses, and projected efficiency versus ϕ for Topology B in the soft-switching region of operation. V_I=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V.

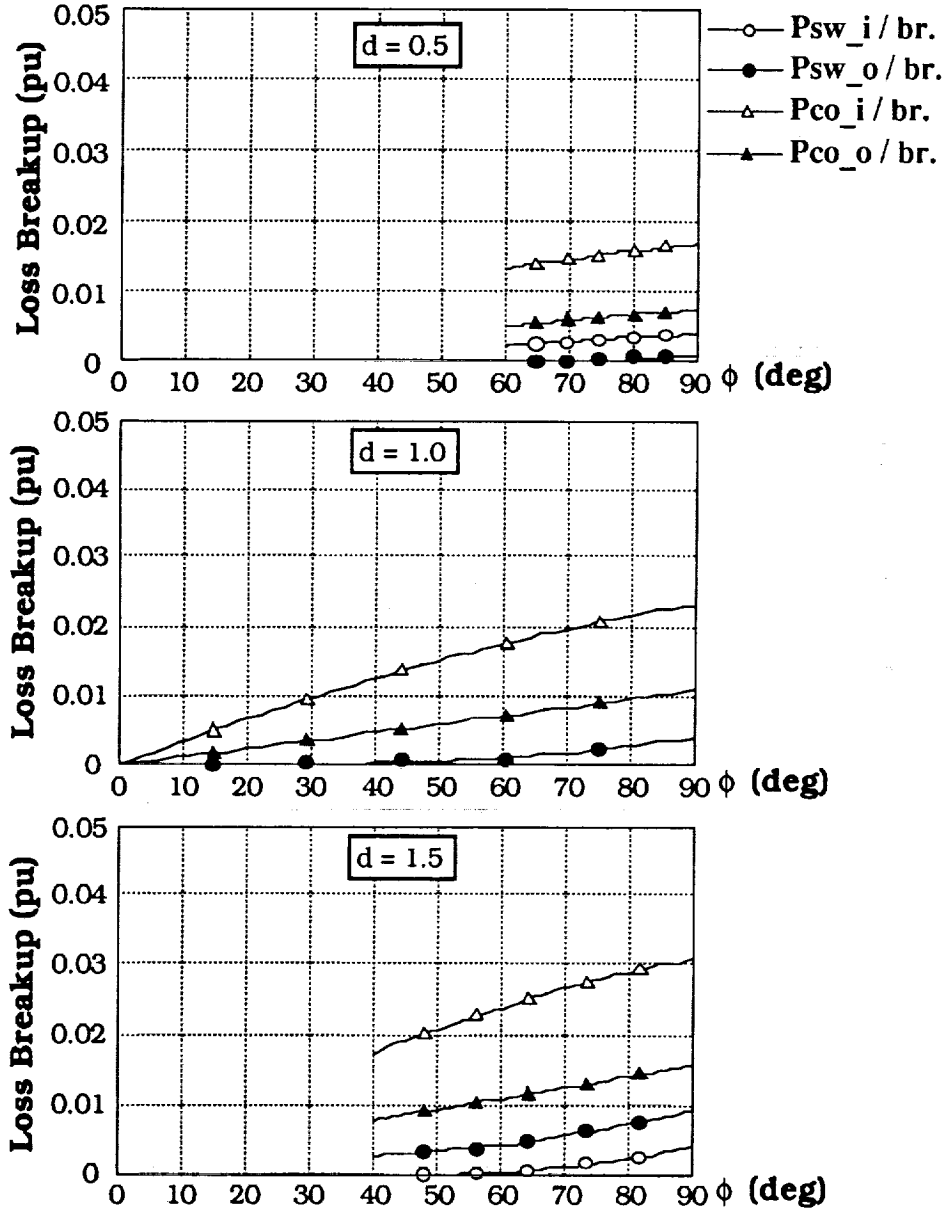


Fig. 4.3.5 Device (IGBT) Loss breakup versus ϕ, for the input and output bridges of Topology C in the soft-switching region of operation. V_i=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V.

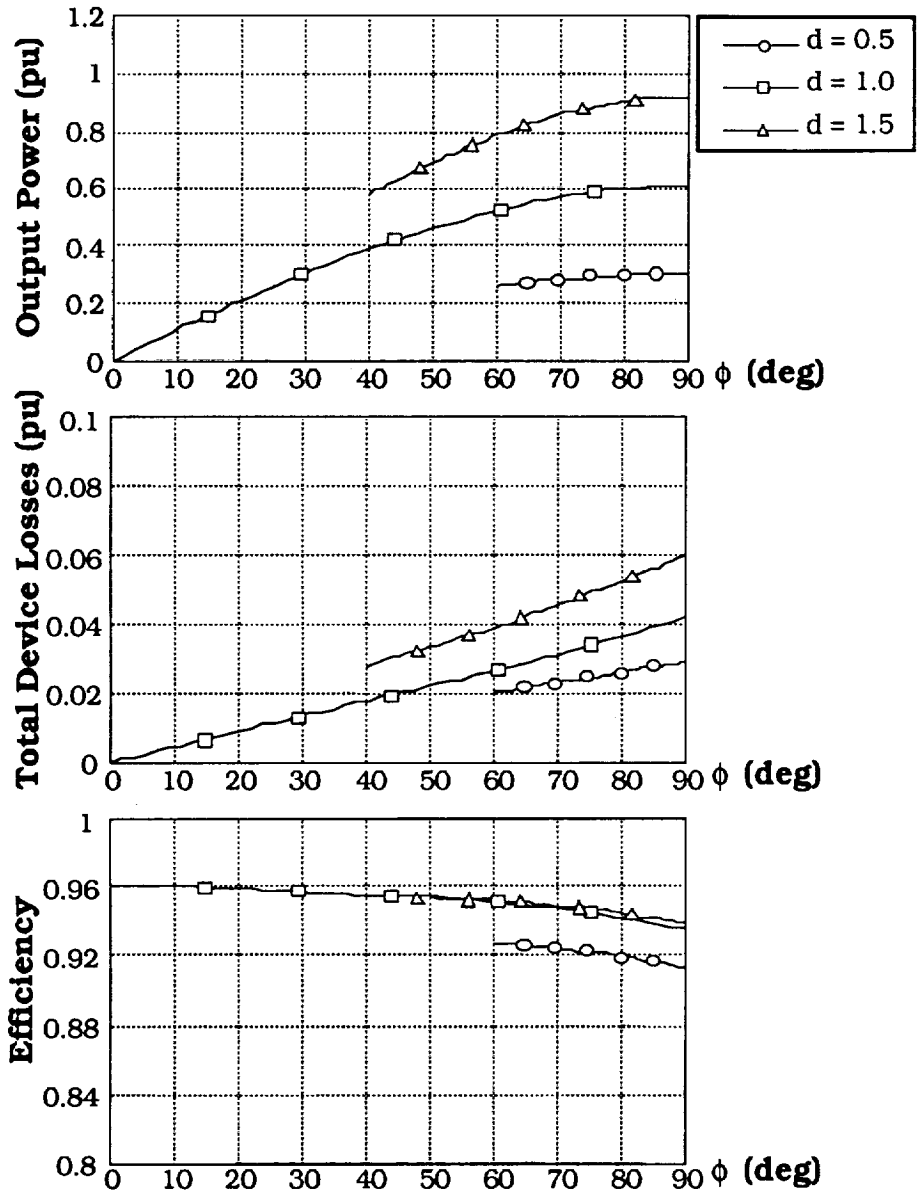


Fig. 4.3.6 Output Power, total device losses, and projected efficiency versus ϕ for Topology C in the soft-switching region of operation. V_i=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V.

the switching cycle. Fig. 4.3.4b indicates that the estimated efficiency drops with decreasing d, because of the reduced power transfer.

As expected, the trend in the converter loss results of Topology C, Figs. 4.3.5, 4.3.6a,b, are identical to those of Topology B. Hence, similar observations can be drawn. However, it is seen that for a given input dc voltage, switching frequency and transformer leakage inductance, Topology C exhibits lower converter losses compared to Topology B, for all values of d. This is a consequence of lower peak currents resulting from three-phase operation.

4.4 Simulated Device Losses for Topology B

As stated in the last section the computed losses are based on the assumption that the duration of the switching transition is negligible compared to the device conduction time. Moreover, the output power and efficiency are also computed based on the idealized analysis of Chapter 3. To ascertain how good an estimate, the computed losses and hence efficiency are, the dual bridge converter (Topology B) is simulated with the actual device (IGBT) turn-off characteristics. Note, the stray inductances in the device package (if any), diode reverse recovery effects are not accounted for. The finite device switching times are incorporated in the simulation. The device parameters (tail time, K, forward drop), snubber capacitances,

transformer turns-ratio (unity) and leakage inductance, and operating conditions are maintained the same as in the analysis.

Various simulated converter waveforms for d=1 and ϕ=60° are shown in Figs. 4.4.1a, b showing the resonant voltage transitions in the presence of finite device snubber capacitances (vp, vs' are primary and secondary transformer voltages, ip is the transformer primary current, Ii and Io' are the input and output bridge currents, IT1_i (ID1_i) is the input bridge device#1 (diode#1) current, IT1_o (ID1_o) is the output bridge device#1 (diode#1) current. Refer to Fig. 3.3.1a). Simulated waveforms for d=0.5, d=1.5, ϕ=60° are shown in Appendix B. All devices are operating near zero-voltage switching conditions.

Fig. 4.4.2 shows a plot of the simulated total device losses for d = 1, with the control parameter, ϕ, swept over the allowable region of soft-switching (note, as will be shown in Chapter 6 the region of soft-switching diminishes under the influence of finite snubber capacitance). A plot of the computed losses is also overlaid for comparison. It is seen that the simulated total devices losses are slightly lower than the computed losses, because the finite device switching times are not ignored. This reflects in the lower device conduction losses. However, if the ESR conduction losses in the snubber capacitor are accounted for (during the resonant transitions) then the simulated losses would increase. The simulated and computed output power are almost identical. The improvement in

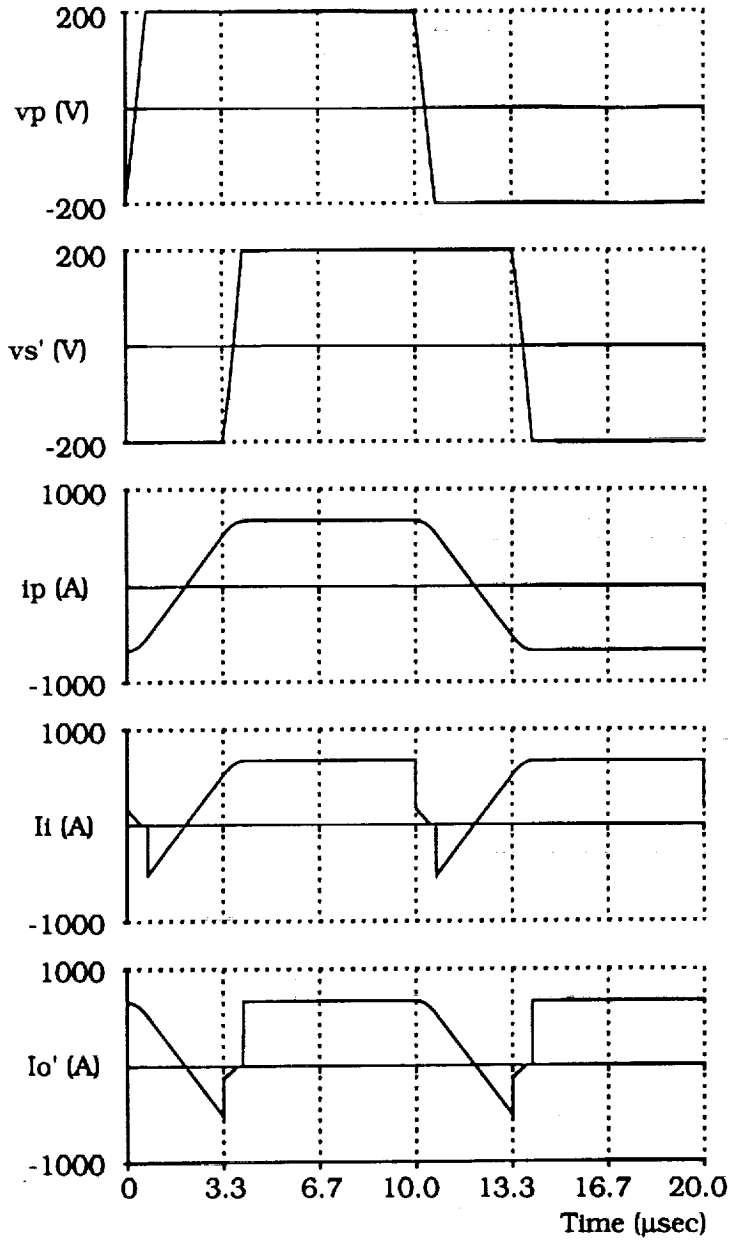


Fig. 4.4.1a Simulated Topology B waveforms showing resonant voltage transitions during device turn-off, with the device(IGBT) turn-off model. d=1, ϕ=60°, V_i=200Vdc, f=50kHz, t_f=0.5µs, K=0.25, V_D=1V, V_T=3V, C_i = C_o = 1µF (input and output snubber capacitors), L = 1µH.

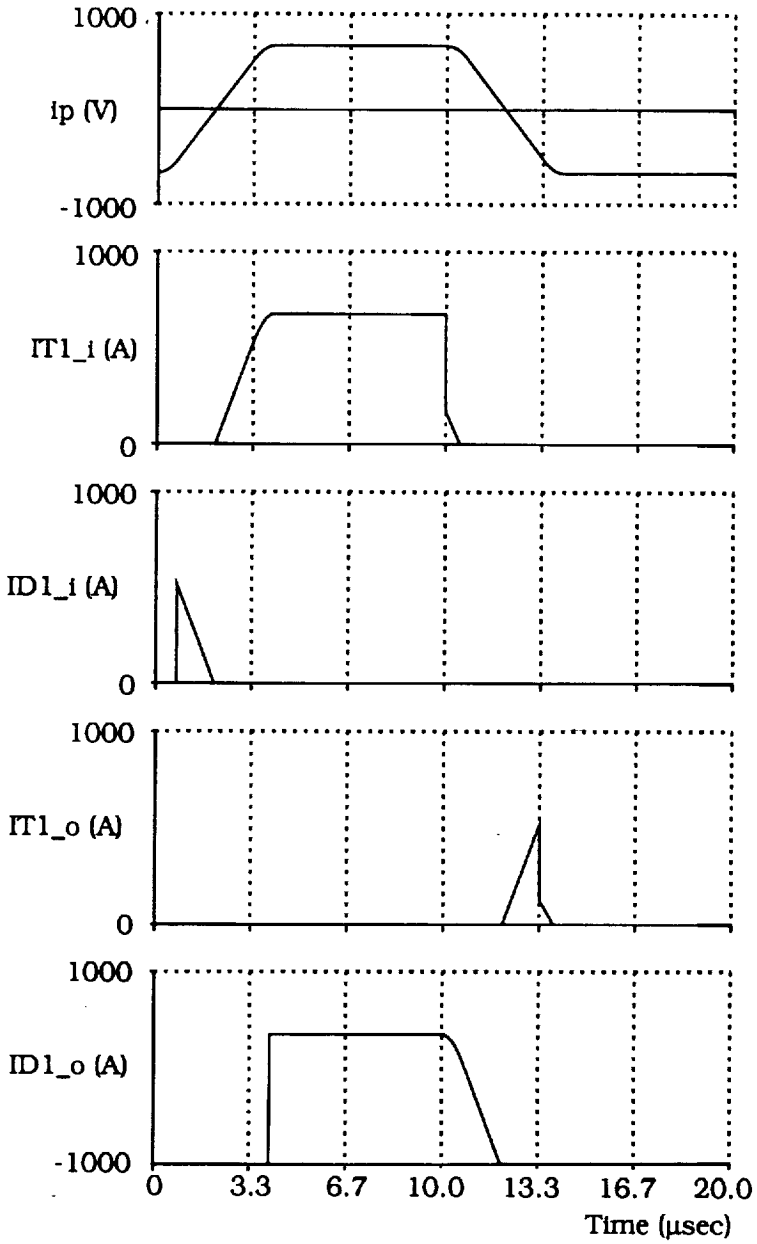


Fig. 4.4.1b Simulated input and output device/diode current waveforms for Topology B, with the device(IGBT) turn-off model. d=1, ϕ=60°, V_i=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V, $C_i = C_o$ = 1μF (input and output snubber capacitors), L = 1μH.

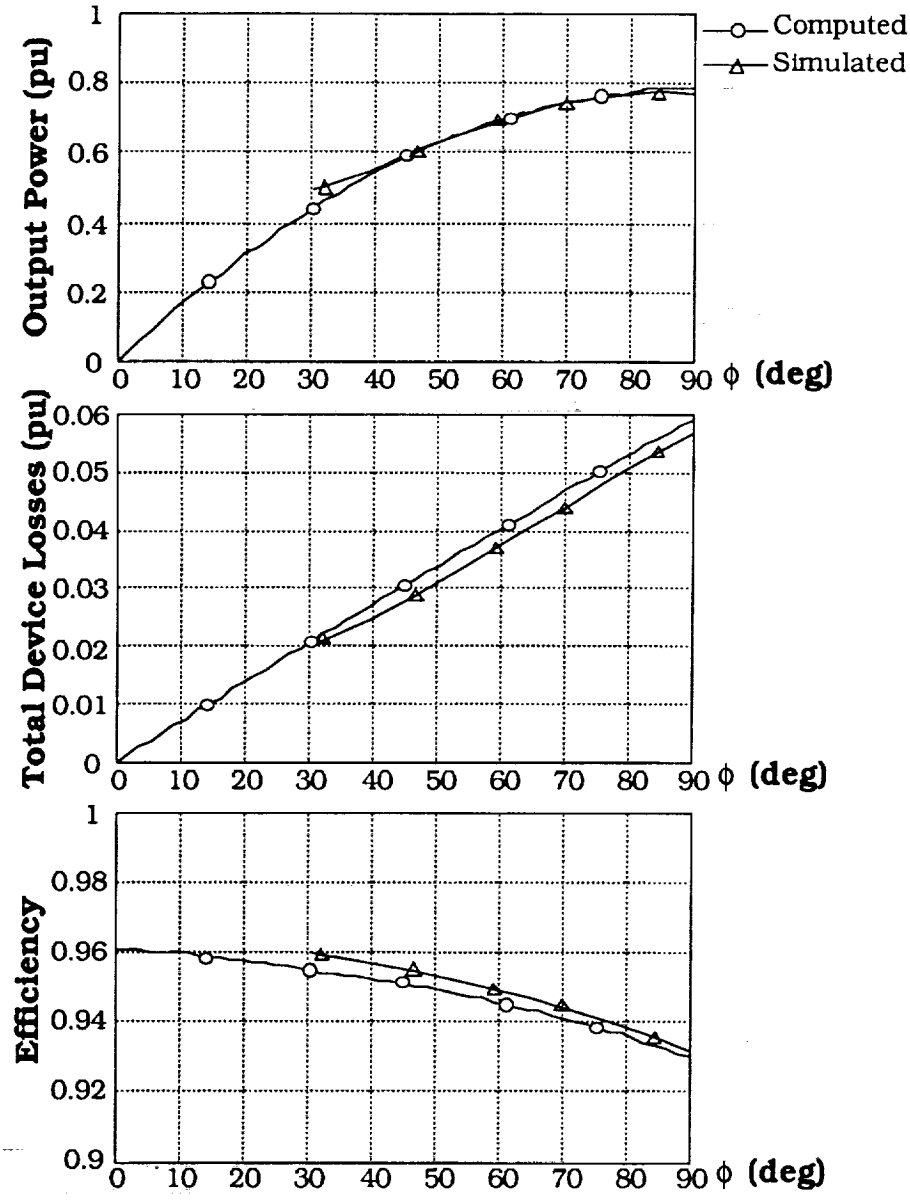


Fig. 4.4.2 Simulated vs. Computed: Output Power, total device losses, and projected efficiency versus ϕ for Topology B in the soft-switching region of operation, for d=1. V_I=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V, $C_i = C_o$ = 1μF, L = 1μH.

projected efficiency is also quite insignificant.

4.5 Summary

A detailed device loss analysis for the three proposed topologies is presented. The dependence of the converter switching and conduction losses, for the IGBT device, on the load and control parameters is shown. Comparison of the computed and simulated device losses for Topology B show little discrepancy. It is thus intended that the designer can use the analytical results to evaluate on a first-cut approach the relative losses and efficiencies in the three proposed schemes.

CHAPTER 5

SELECTION OF FINAL CONVERTER TOPOLOGY

5.1 Introduction

Based on the knowledge of the performance characteristics of the active and passive components in the three proposed topologies, presented so far, we are now in a position to quantitatively assess the merits and demerits of these circuits. The final objective is to select one of these topologies which realizes the highest power density, for the given rated specifications, under minimal component stresses, device losses and control complexity. These issues are investigated based on the consideration that each topology operates at its optimum transformer utilization at rated conditions of 50 kW, input dc voltage of 200V, output dc voltage of 2000V and a minimum switching frequency of 50 kHz.

5.2 Component Stress Comparison

Since high power density is the most stringent requirement, and the transformer is the biggest component in the system, it seems reasonable to design the circuit based on an optimum transformer utilization. For Topology A, this optimum operating

point (see point labelled X on Fig. 3.2.4b) is the minimum transformer kVA (0.475 pu) required to transfer the maximum power (0.302 pu). This corresponds to a phase-shift, $\beta = 180°$ and d = 0.58. As observed in Chapter 3, Topology B gives a 40% improvement in the transformer utilization over that of Topology A for the same transformer kVA of 0.475 pu at d = 1, by virtue of an active output bridge. Hence, for purpose of comparison, this seems like a reasonable operating point (see point labelled X in Fig. 3.3.4b) for Topology B. The corresponding phase-shift, ϕ, turns out to be 28.8°. For Topology C, a similar design philosophy of choosing an operating point for d = 1 (see point labelled X in Fig. 3.4.4b), corresponding to the minimum transformer kVA required for the maximum power transfer on its output constraint (i.e., diode bridge constraint), leads to a design point corresponding to a $\phi = 35.4°$.

The next step is to evaluate the various quantities related to the switching devices, filters and transformer, for each topology operating at its selected optimum operating point. These quantities are denormalized to conform to the given rated specifications and are tabulated in Table 5.2.1.

Examining the peak device stresses for each bridge, Topology C offers the lowest ($V_{pk} * I_{pk} / P_o$) stress at 1.17 pu. However, Topology B shows a slightly higher stress of 1.19 pu, with a saving of two devices on each bridge. Topology A exhibits very high device stresses on both the bridges. In fact, the 1.19 pu device stress for

Topology B compares favourably with the desired stress of 1 pu, theoretically achievable with hard-switched pwm converters.

Comparing the transformer specifications, again Topology A seems to be the poorest with regard to peak current stresses and transformer utilization. Both Topologies B and C offer almost identical performances. However, it must be emphasized that Topology C requires a three-phase transformer with identical equivalent leakage inductances in each phase. This is necessary for two reasons :

(i) Balanced three-phase currents, resulting in current components at multiples of six times the switching frequency only, at the dc sides of the bridges. Hence, reduction in the r.m.s. current ratings of the filter capacitors, and

(ii) The minimum current constraint for zero-voltage switching of the active devices at turn-off, is dictated by the value of the leakage inductance and snubber capacitance. Hence, for this minimum current to be identical for each device, it is necessary that the leakage inductance be identical in each phase.

Fig. A.1 (Appendix A) shows a possible construction of such a symmetrical three-phase transformer. In view of the constraint of high power density, the non-conventional core geometry requiring additional yokes could be a challenging problem to resolve.

Table 5.2.1

(Summary of Component Stresses)

(P_O = 50 kW ; V_i = 200 Vdc ; V_O = 2000 Vdc ; f = 50 kHz)

	Topology A	**Topology B**	**Topology C**
d	0.58	1.0	1.0
β (°)	180	-	-
ϕ (°)	-	28.8	35.4
Device Specifications for Input Bridge			
Active devices	4	4	6
Vpk (V)	200	200	200
Ipk (A)	861.5	297.6	293.5
Vpk * Ipk / Po	3.45	1.19	1.17
Device Specifications for Output Bridge			
Active devices	4 diodes	4	6
Vpk (V)	2000	2000	2000
Ipk (A)	50.7	29.8	29.4
Vpk * Ipk / Po	2.03	1.19	1.17
Transformer Specifications			
Npri : Nsec	1 : 17	1 : 10	1 : 10 (Y-Y)
Pri. Vpk (V)	200	200	133 / ph
Pri. Ipk (A)	861.5	297.6	293.5
Pri. Irms (A)	497.5	281.4	197.3 / ph
Sec. Vpk (V)	2000	2000	1333 / ph
Sec Ipk (A)	50.7	29.8	29.4
Sec Irms (A)	29.3	28.1	19.7 / ph
kVA	78.6	56.3	55.7
Po / kVA	0.64	0.89	0.89
L (μH)	0.77	1.1	0.89 / ph
Input Filter Capacitor Specifications			
Cap. Irms (A)	429.8	129.2	48.4
Cap. kVA	86.0	25.8	9.7
Output Filter Capacitor Specifications			
Cap.Irms (A)	14.6	12.9	4.8
Cap. kVA	29.3	25.8	9.7

Finally, examining the input and output filter capacitor ratings, Topology C exhibits the lowest r.m.s. current stresses and hence, lowest kVA, for reasons mentioned above. Topology A is the worst with 9 times the kVA rating for that of the input capacitor for Topology C. However, the output filter stresses for Topology A are much lower compared to its input filter. This is because, the output bridge being a diode bridge allows the current on its dc side to be unidirectional only, resulting in lower ripple currents.

5.3 Converter Loss Comparison

Table 5.3.1 summarizes the total projected switching and conduction loss figures for the three topologies at the rated output power of 50 kW, switching at 50 kHz for both the IGBT and MCT [28]. These figures are evaluated at the design points selected in Table 5.2.1 (for stress comparison). The losses are computed based on the assumptions and analysis presented in Chapter 4. For each topology the snubber capacitors are designed for critical snubbing at the worst case (maximum turn-off current) operation. This ensures that under normal range of operation the device is reasonably oversnubbed, as desired. The device turn-off profile is assumed identical for the two device types, with a fall time, t_f, approximated essentially as the tail time. t_f is selected as 0.5 μs and K as 0.25 from references [26,27]. IGBT's have substantially higher on-state voltages

Table 5.3.1

(Comparison of Projected Semiconductor Losses)

(P_o = 50kW, V_i = 200 Vdc, V_o = 2000Vdc, f = 50kHz)

(IGBT: V_T = 3V, V_D = 1V, t_f = 0.5μs, K = 0.25)

(MCT: V_T = 1.4V, V_D = 1V, t_f = 0.5μs, K = 0.25)

	Topology A		**Topology B**		**Topology C**	
	IGBT	MCT	IGBT	MCT	IGBT	MCT
Switching Loss (W)	442	442	143	143	105	105
Conduction Loss (W)	2283	1192	1619	795	1667	818
Total Loss (W)	2725	1634	1762	938	1772	923

than MCT's thus resulting in higher conduction losses. With on-state voltages of 1.4V, assumed for the MCT [27], a 50% reduction in the conduction losses is seen for all the topologies. The highest conduction losses, incurred by Topology A, is a consequence of its highest current stresses.

5.4 Final Topology

Of the three proposed topologies, B and C possess the following desirable attributes :

1) Good range of control, especially for a dc conversion ratio (d) of unity.

2) Buck/boost operation.

3) High transformer utilization.

4) Low device and transformer stresses.

5) Bi-directional power flow.

However, bearing in mind the requirement of high power density, Topology C suffers in the following aspects :

1) Requires 4 additional devices (2 on each bridge), with its associated gate-driver circuits. Moreover, the requirement of high voltage on the output side, thus mandating multiple series

connected switches or multiple series connected bridges puts a heavy demand on the realization of high power density and reliability.

2) Complex transformer construction, with a weight penalty associated with the additional yokes required for symmetry (Fig. A.1).

Topology C shows a distinct advantage over Topology B, with its lower filter kVA-ratings. However, state-of-the-art multi-layer ceramic capacitors (MLC) offer much higher power densities than conventional commutation-grade or electrolytic capacitors. The total weight required for the filter capacitors for Topology B is thus seen to be only marginally higher than that for Topology C.

From a consideration of the above arguments Topology B offers the most desirable characteristics. Further, from the converter loss analysis, it is seen that topologies B and C incur very similar losses at their optimum design points.

Since the control methodology for Topology A can be incorporated in Topology B, a wider range of control is possible by superimposition of their V_O' - I'_O characteristics, as shown in Fig. 5.4.1. It should be remembered that the $\beta = \pi$ boundary for Topology A is identical to the diode bridge constraint for Topology B. Transitioning from operation in Topology B mode to A mode effectively extends the soft-switching range of the converter. A significant implication of this is that the load current could be held

constant even under short-circuit faults, and with all the devices always operating under soft-switching conditions.

The features of Topology B make it the most desirable choice as the final topology. The issue of the concept being extendible to megawatt power levels is next addressed. Given the high power density constraint, it is not possible to use conventional Gate Turn Off (GTOs) devices at the high frequency required. The most suitable approach seems to be the use of modules individually rated at 50-100kW using IGBT or MCT devices with ratings of approximately 1200V, 400A (at least on the input side).

Two alternate schemes possible involve paralleling or series connection of the modules. However, as output voltages needed are in the multi-kilovolt range, the use of passive diode rectifiers and a parallel connection causes problems as diodes are fairly slow. The use of series connected bridges, with active devices, thus becomes a reasonable approach if high power density constraint is to be simultaneously met. For the specified output voltage(2000Vdc) and devices rated at 1200V a series connection of two active half-bridges (on the output side), as shown schematically in Fig. 5.4.2, is implemented. The design, control and layout issues are addressed in the experimental chapter.

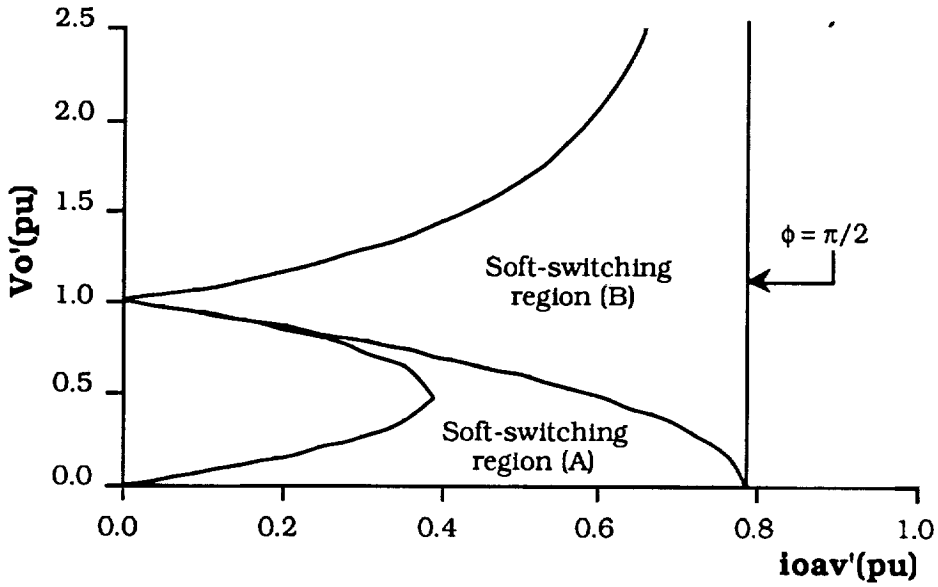


Fig. 5.4.1 Extension of soft-switching region of Topology B, by operating in Topology A mode.

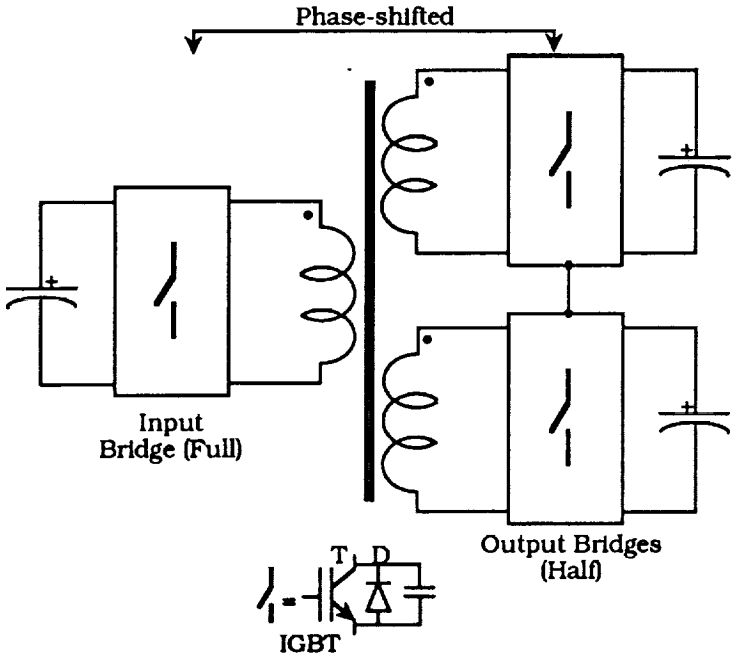


Fig. 5.4.2 Series connection of output half-bridges for high voltage outputs (Topology B).

5.5 Summary

A detailed stress and loss analysis for the three candidate topologies is presented. Based on the analysis and considerations of high power density and good controllability, Topology B is the most desirable choice for the application. For power levels in the megawatt range, a modular approach must be adopted for high power densities. Further, the multi-kilovolt output requirement mandates a cascade connection for the output active bridges.

CHAPTER 6

SOFT-SWITCHING OPERATION IN THE PRESENCE OF DOMINANT PARASITICS

6.1 Introduction

Having established the operation of the proposed idealized converter topologies from a simplified steady state analysis, it is now appropriate to relax some of the assumptions, in particular with regard to the dominant parasitics such as the transformer magnetizing inductance and device snubber capacitance, and to study their influence (independent of each other) on the converter performance. The purpose of this exercise is to ascertain the change in the soft-switching region, if any. A detailed analysis is carried out for the selected converter topology B [29]. The results are then extended to topology A.

6.2 Influence of Magnetizing Inductance (Topology B)

Fig. 6.2.1 shows the primary referred model for the converter with the input and output bridges replaced by square wave voltage sources. The T-model has been assumed for the transformer, with half the leakage inductance shown on each side of the finite magnetizing inductance. It is valid to assume that the winding

resistances are negligible compared to the leakage reactance at the high frequencies of interest.

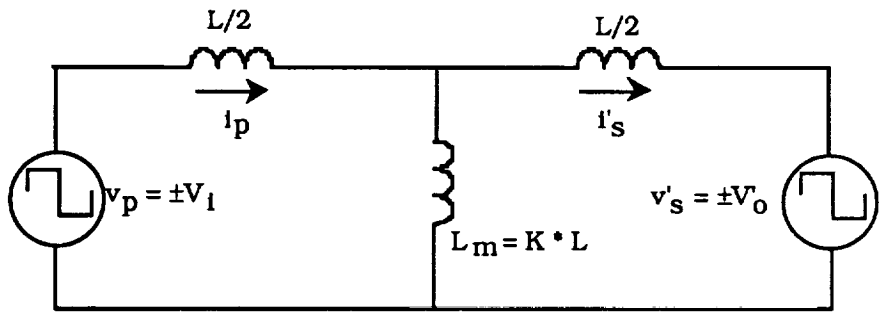


Fig. 6.2.1 Primary-referred model of Topology B, with T-model for the transformer.

The snubber capacitances across the devices are assumed to be negligible. The foregoing analysis is carried out for forward power transfer with the input bridge phase-leading the output bridge. Let the magnetizing inductance, L_m, be equal to K*L, where L is the total leakage inductance and $K \geq 1$. Defining v_m as the voltage across L_m, we can then write i_p, i_s' (note, all variables reflected onto the primary side of the transformer are with primes) and i_m as,

$$\frac{di_p}{d\theta} = \frac{v_p - v_m}{\frac{\omega L}{2}} \qquad \ldots(6.2.1)$$

$$\frac{di_s'}{d\theta} = \frac{v_m - v_s'}{\frac{\omega L}{2}} \qquad \ldots(6.2.2)$$

$$\frac{di_m}{d\theta} = \frac{v_m}{\omega L_m} \qquad \ldots(6.2.3)$$

Note that v_p, v_s', v_m, i_p, i_s', i_m are functions of θ, where $\theta = \omega t$, and ω is the switching frequency in radians/sec. Moreover,

$$i_m = i_p - i_s' \qquad \ldots(6.2.4)$$

Eliminating i_m from eqns. (6.2.1)-(6.2.4) and carrying out the necessary algebra,

$$\frac{di_p}{d\theta} = K_1 v_p - K_2 v_s' \qquad \ldots(6.2.5)$$

$$\frac{di_s'}{d\theta} = K_2 v_p - K_1 v_s' \qquad \ldots(6.2.6)$$

$$v_m = \frac{1}{2 + \frac{1}{2K}}\left[v_p + v_s'\right] \qquad \ldots(6.2.7)$$

where,

$$K_1 = \frac{1 + \frac{1}{2K}}{\omega L(1 + \frac{1}{4K})} \qquad \ldots(6.2.8a)$$

$$K_2 = \frac{1}{\omega L(1 + \frac{1}{4K})} \qquad \ldots(6.2.8b)$$

Again, two modes of operation (for each half-cycle) can be identified for the converter. Evaluating the current i_p in each mode and using the half-wave symmetry conditions,

$$i_p(0) = -V_i K_2 \left[d\phi + \frac{\pi}{2} \left(\frac{K_1}{K_2} - d \right) \right] \qquad \ldots(6.2.9)$$

where,

$$d = \frac{V_o'}{V_i}$$

and, V_i is the input dc voltage, and V_o' is the primary referred output dc voltage. Enforcing the soft-switching constraint for the input bridge devices,

$$i_p(0) \leq 0$$

we get from eqn. (6.2.9),

$$d \leq \frac{K_1}{K_2}\left[\frac{\pi}{\pi - 2\phi}\right] \qquad 0 \leq \phi \leq \frac{\pi}{2} \qquad \ldots(6.2.10)$$

Similarly, from the modal analysis for i_s' and the soft-switching constraint for the output bridge,

$$i_s'(\phi) \geq 0$$

$$d \geq \frac{K_2}{K_1}\left[1 - \frac{2\phi}{\pi}\right] \qquad 0 \leq \phi \leq \frac{\pi}{2} \qquad \ldots(6.2.11)$$

Note, as L_m tends to infinity (i.e. K tends to infinity), eqns. (6.2.10) and (6.2.11) reduce to eqns. (3.3.7) & (3.3.8) respectively. The average output current, I_o', can be evaluated by taking the average of the product of i_s' and the output bridge switching function. This simplifies to,

$$I_o' = V_i \, \phi \, K_2\left[1 - \frac{\phi}{\pi}\right] \qquad \ldots(6.2.12)$$

Hence, the output power, P_o, is given as,

$$P_o = V_o' \, I_o'$$

$$= \frac{V_i^2}{\omega L} d\phi\left[1 - \frac{\phi}{\pi}\right]\left[\frac{1}{1 + \frac{1}{4K}}\right] \qquad \ldots(6.2.13)$$

Note, as K tends to infinity, P_o reduces to the idealized output power expression derived in eqn. (3.3.10).

To illustrate the influence of the magnetizing inductance, the output power as derived in eqn. (6.2.13) is plotted as a function of ϕ, for two values of K, with d set to unity. Fig. 6.2.2 shows this plot with the soft-switching boundaries also evaluated for the same values of K. The soft-switching boundaries are given in eqns. (6.2.10) and (6.2.11). $K = \infty$ represents an infinite value of the magnetizing inductance (ideal case). K = 1, although not realistic, represents the other extreme for the magnetizing inductance. As K increases the soft-switching boundaries come closer, thus shrinking the desired region of soft-switching. This is seen to be reasonable because with decreasing magnetizing inductance, the load appears more lagging which, as stated earlier, is a precondition for zero-voltage switching. Also, as illustrated for the case d = 1, the maximum power transferred to the output decreases with decreasing K. The penalty for lower magnetizing inductance is thus, low transformer utilization.

Fig. 6.2.3 shows the soft-switching region on the V_O'- I_O' plane for the same two values of K. It is seen that for low values of the output current, the region of soft-switching widens as K decreases. This result can be used to advantage for applications requiring voltage control at lightly loaded conditions. On the other hand, the maximum average output current, governed by the $\phi = \pi/2$ boundary (explained in Chapter 3), diminishes with decreasing K. The parameter K is a mechanism for trading of range over d achievable under soft switching.

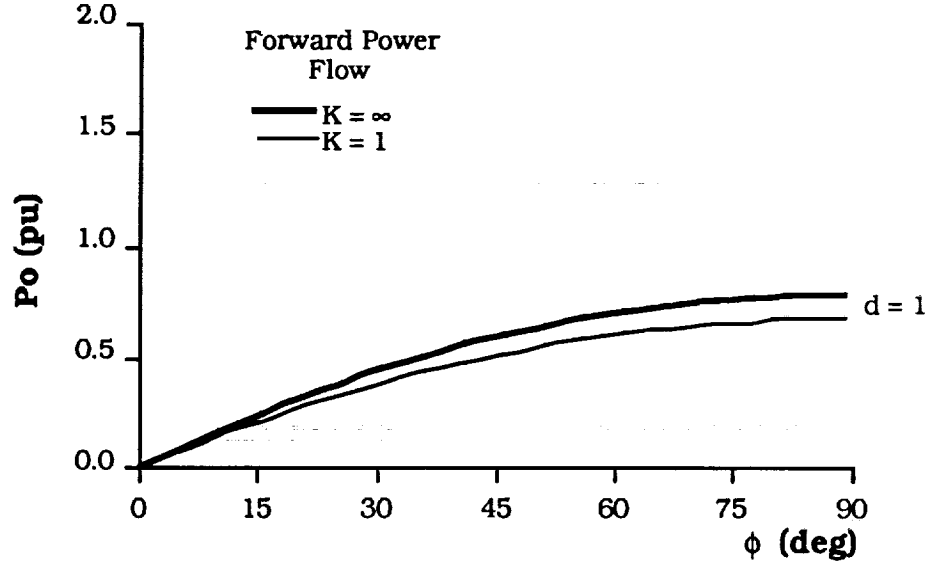


Fig. 6.2.2 Influence of transformer magnetizing inductance on the output power transfer, for Topology B. $K = L_m / L$.

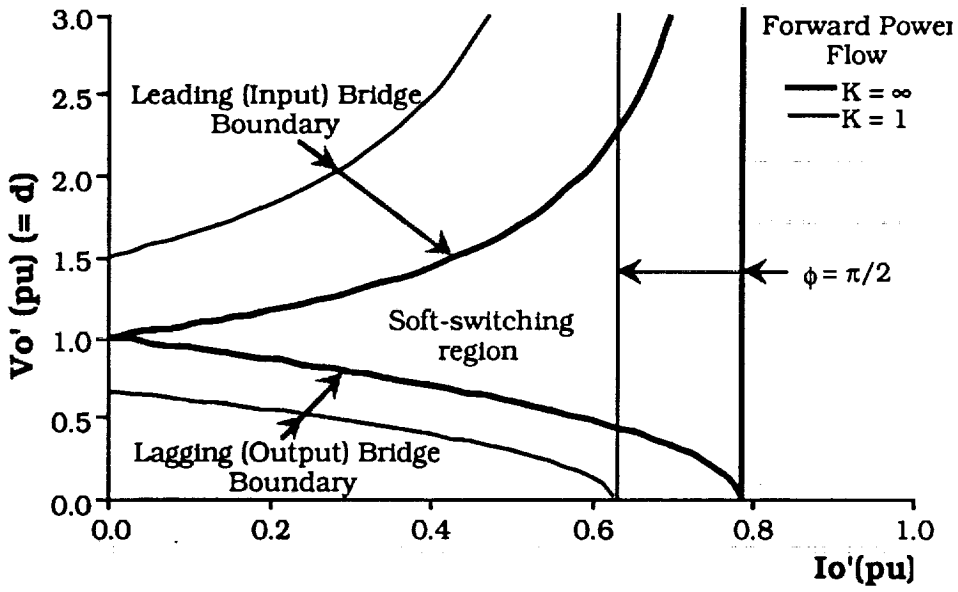


Fig. 6.2.3 Influence of transformer magnetizing inductance on the output voltage-output current plane, for Topology B. $K = L_m / L$. The widening of soft-switching region is shown as K is reduced to 1 (an exaggerated case).

6.3 Influence of Snubber Capacitance (Topology B)

The purpose of this section is to study the influence of snubber capacitance on the minimum current required at instant of turn-off of any of the devices on either of the input or output bridges. The derivation of the soft-switching regions from the steady state analysis of the proposed topologies, in Chapter 3, was carried out under the assumption that the minimum current required is zero. Although not a very realistic assumption, it was necessary to do so, to ascertain the fundamental working principle of the proposed converters from a simplified analysis. It is shown here that with increasing values of snubber capacitance, the minimum current required for zero voltage switching of any of the devices increases. This further restricts the region available for soft-switching on the output voltage versus output current plane.

Fig. 6.3.1a shows the input bridge. L is the leakage inductance of the transformer (magnetizing inductance is assumed infinite). C1 and C2 are the snubber capacitances for the input bridge devices, T1 (T4) and T2 (T3). Note, C1 = C2. The influence of snubber capacitance on the minimum current required to flow through L for zero-voltage switching on the input devices is investigated. The analysis is for the case where the input bridge is phase-leading the output bridge. Moreover, even though the analysis is done for a switching event on the input bridge, the results hold for any switching event on the output bridge also, provided the two events

do not overlap (which would violate the soft-switching constraints).

Let us assume that at t = 0, the device T1 (T4) turn-off, as shown in Fig. 6.3.1b. All other devices, shown in Fig. 6.3.1a, are not conducting at this instant of time. The turn-off time of the device is considered negligible, and the value of C1 (or, C2) sufficiently large to ensure very little change in the voltage across T1 during its turn-off time. Once the device turns off, the current in L discharges C2 and charges C1 in a resonant manner, until their respective voltages reach the opposite rails at which point of time, if the current is still positive, diode D2 (D3) turn on clamping the voltage across C2 to zero and that of C1 to V_i. The current, i_p, through L is in the direction shown in Fig. 6.3.1a. The output bridge is replaced by a primary-referred voltage source, V_o', with the polarity required during this event. We need to find the minimum i_p at t = 0, which ensures that the voltage across T1 (T4) reaches the clamping value (V_i) when i_p reaches zero. Let $t = t_m$ be the instant of time at which i_p just reaches zero. Hence, at t = 0,

$$i_p = I_{min} ; \qquad v_{C1} = 0 ; \qquad v_{C2} = V_i ;$$

and, at $t = t_m$

$$i_p = 0 ; \qquad v_{C1} = V_i ; \qquad v_{C2} = 0 ;$$

During, the interval $0 \le t \le t_m$,

$$i_p = C1 \frac{dv_{C1}}{dt} + C2 \frac{dv_{C2}}{dt} \qquad \ldots(6.3.1)$$

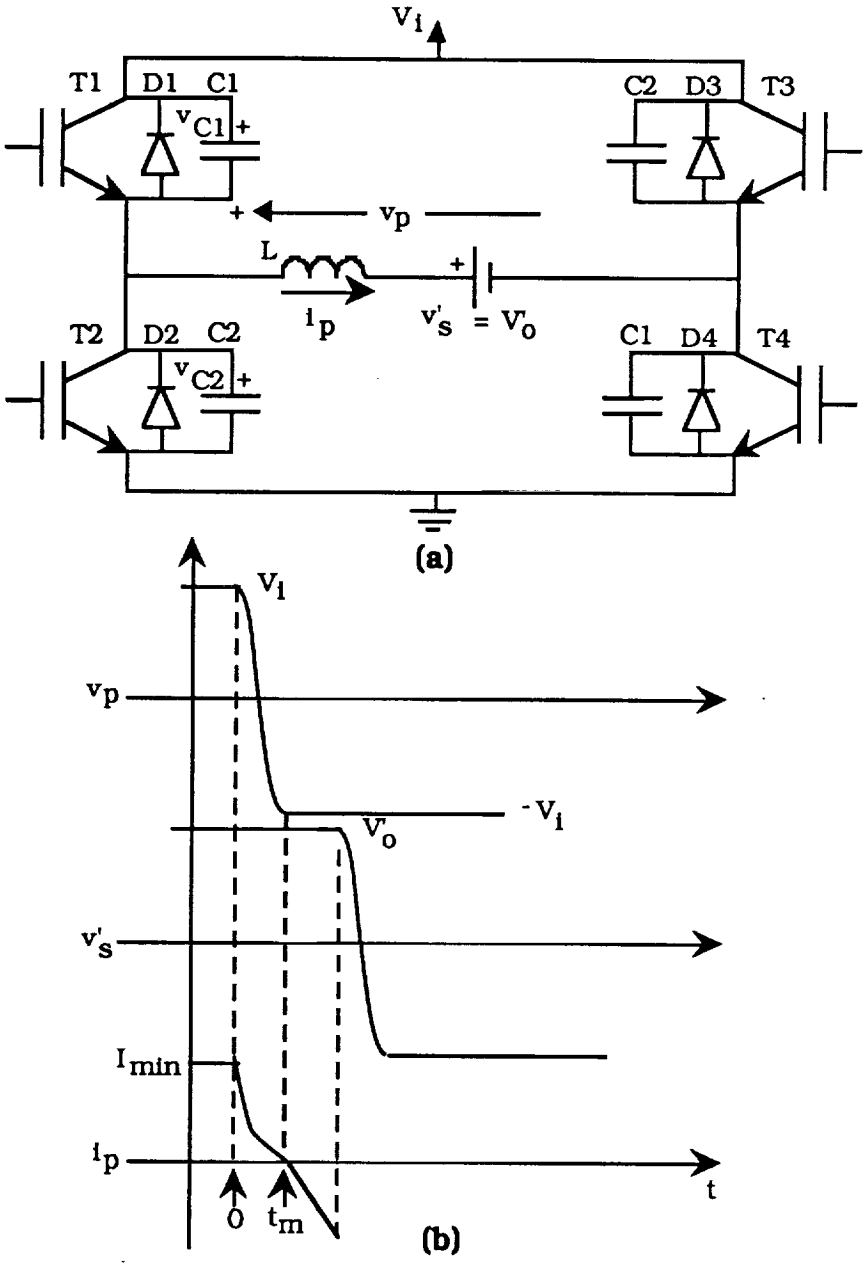


Fig. 6.3.1 (a) Topology B shown with the output bridge replaced by an equivalent voltage source during turn-off of devices T1 (T4) of input bridge. (b) Minimum inductor current required at instant of turn-off of T1 (T4), to resonate the pole voltage from $+V_i$ to $-V_i$.

Since, C1 = C2 = C

$$\frac{dv_{C1}}{dt} = \frac{dv_{C2}}{dt} = \frac{dv_C}{dt} \text{ (say)} \qquad \ldots(6.3.2)$$

Hence, from eqns. (6.3.1) and (6.3.2), we get,

$$i_p = 2C \frac{dv_C}{dt} \qquad \text{during } 0 \le t \le t_m \qquad \ldots(6.3.3)$$

From Energy Balance considerations,

$$E(t = 0) = E(t = t_m) + E_{loss} + E_{delivered}$$

Assuming, lossless circuit elements,

$$\frac{1}{2} L I_{min}^2 + \frac{1}{2} C2 V_i^2 = \frac{1}{2} C1 V_i^2 + E_{delivered} \qquad \ldots(6.3.4)$$

$$E_{delivered} = \int_0^{t_m} V_o' i_p \, dt$$

Substituting for i_p from eqn. (6.3.3),

$$E_{delivered} = 2CV_o' \int_0^{t_m} v_C$$

Zero voltage switching condition, dictates that the $dv_C = V_i$ during the interval $0 \le t \le t_m$, Hence,

$$E_{delivered} = 2CV_o'V_i \qquad \ldots(6.3.5)$$

Putting C1 = C = C2, and substituting $E_{delivered}$ from eqn. (6.3.5), into eqn. (6.3.4), we get,

$$I_{min} = \frac{1}{Z_o}\sqrt{2\,V_i\,V_o'} \qquad \text{where, } Z_o = \sqrt{\frac{L}{C}} \qquad \ldots(6.3.6)$$

Normalizing I_{min} with respect to $\frac{V_i}{\omega L}$ and defining,

$$\omega_o = \frac{1}{\sqrt{L\,C}}$$

$$I_{min(pu)} = \frac{2}{\omega_n}\sqrt{d} \qquad \ldots(6.3.7)$$

where,

$$d = \frac{V_o'}{V_i}; \qquad \omega_n = \frac{\omega_o}{\omega}$$

and, ω is the switching frequency in radians/sec.

Fig. 6.3.2 shows a family of curves of $I_{min(pu)}$ versus d with ω_n as the parameter. For a given value of L, ω and d, I_{min} increases, as C increases. Also, for a fixed value of L, ω and C, I_{min} increases as d increases.

For any given operating condition (except for d = 1), only one of the two bridge devices must satisfy the minimum current relation at turn-off. For instance, during the buck (d < 1) mode of operation the current at turn-off of the output bridge devices is lower than the current at turn-off of the input bridge devices (assuming a primary-referred circuit). Hence, the current at turn-off of the output bridge devices must at least be equal to I_{min} derived in eqn. (6.3.7).

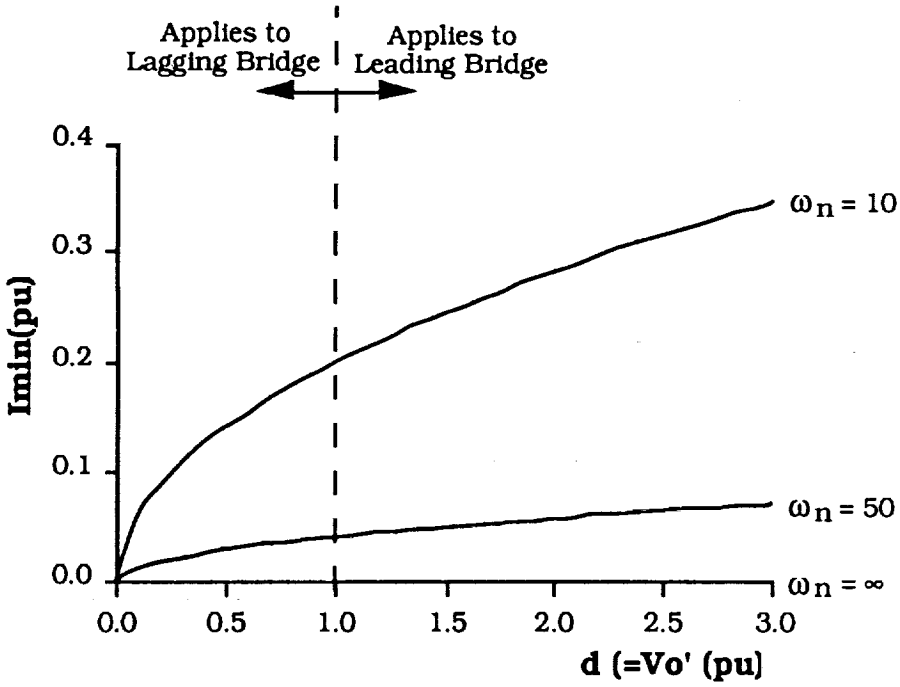


Fig. 6.3.2 Plot of required minimum inductor current (for soft-switching) as a function of d with ω_n as a parameter. For forward power flow input bridge leads the output bridge.

Equating the turn-off current of the output bridge devices, derived in Chapter 3 - Section 3, to eqn. (6.3.7) we can calculate the minimum phase-shift required for lossless turn-off of the output bridge devices for the $d < 1$. Hence, we can now calculate the minimum average output current for all d's less than 1, which gives us the new output bridge soft-switching boundary on the output voltage-output current plane.

Conversely, for the boost ($d > 1$) mode of operation the current at turn-off of the input bridge devices is lower than the current at turn-off of the output bridge devices. Repeating the above analysis, the new input bridge soft-switching boundary on the output voltage-output current plane can be evaluated. For the case $d = 1$ both the bridges must satisfy the minimum current constraint. Hence,

$$\phi_{min}\Big|_{d<1} = \frac{2\sqrt{d}}{\omega_n} + \frac{\pi\,(1-d)}{2} \qquad \ldots(6.3.8a)$$

$$\phi_{min}\Big|_{d\geq 1} = -\frac{1}{d}\left[\frac{2\sqrt{d}}{\omega_n} + \frac{\pi\,(1-d)}{2}\right] \qquad \ldots(6.3.8b)$$

$$\text{Min. } I_o' \text{ (pu)} = \phi_{min}\left[1 - \frac{\phi_{min}}{\pi}\right] \qquad \ldots(6.3.9)$$

Fig. 6.3.3 shows how the soft-switching region reduces on the V_o' - I_o' plane with increasing snubber capacitance (decreasing ω_n). Clearly, the trade-off here is that to reduce switching losses by increasing C the range of control under soft-switching is reduced. However, it should be noted that the decrease in Vo-Io plane due to C can be compensated, at least in part, by the impact of the transformer magnetizing inductance. A good design must take into account all these parameters for high efficiency and wide range of control.

6.4 Influence of Magnetizing Inductance (Topology A)

Using the model of Fig. 6.2.1, eqns. (6.2.1) through (6.2.8) and applying the modal analysis (three modes of operation for half switching period), it can be shown that from the output diode bridge constraint,

$$\phi = \frac{1}{2}\left[\beta - \frac{K_1}{K_2} d\,\pi\right] \qquad \ldots(6.4.1)$$

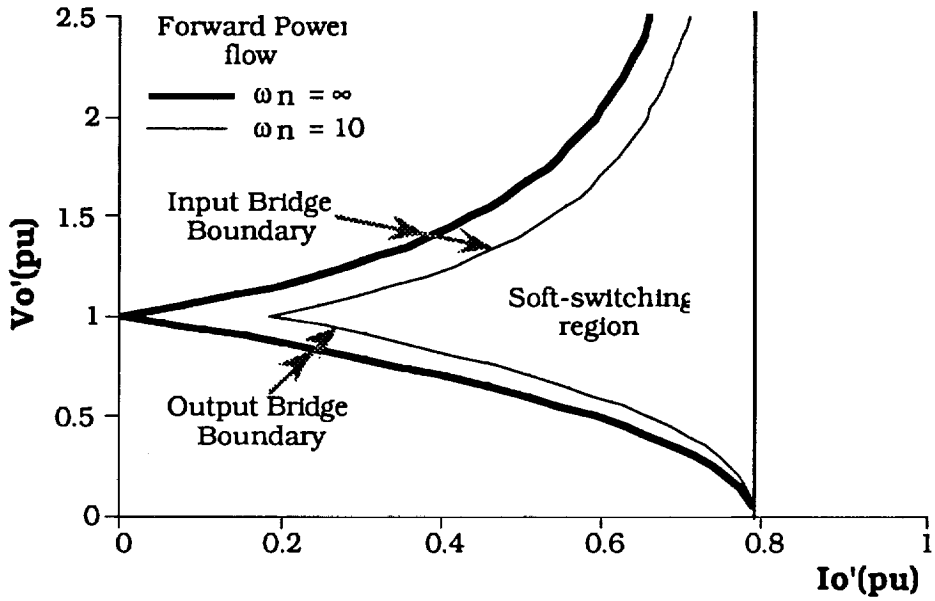


Fig. 6.3.3 Computed plot showing the influence of snubber capacitance on the soft-switching region on the output voltage-output current plane for Topology B. ω_n decreases as snubber capacitance increases.

where, ϕ is the resultant phase-shift between the input bridge and the output diode bridge, and β is the controlled phase-shift between the the two poles of the input active bridge. Enforcing the input bridge soft-switching constraint,

$$d \leq \left[\frac{K_2}{K_1}\frac{(\beta - \pi)}{(2\pi)}\right] + \sqrt{\left[\frac{K_2}{K_1}\frac{(\beta - \pi)}{(2\pi)}\right]^2 + \frac{\beta}{\pi}} \quad \ldots(6.4.2)$$

The average output current of the converter is derived as,

$$I_o' = \frac{V_i}{4\pi} K_2 \left[\beta (2\pi - \beta) - \left[\frac{K_1}{K_2} d \pi\right]^2\right] \quad \ldots(6.4.3)$$

The influence of the magnetizing inductance on the soft-switching region of operation is shown on the computed output voltage - output current plane in Fig. 6.4.1. For an exaggerated case of K = 1 (which implies that the magnetizing and leakage inductances are equal), it is seen that the for heavy loading the soft-switching region is reduced. However, at lightly loaded conditions a relatively wider region of the plane is accessible under soft-switching. Note, also, that the diode bridge boundary is identical to the output bridge boundary of Topology B.

6.5 Influence of Snubber Capacitance (Topology A)

The influence of snubber capacitance on the input active bridge will only be demonstrated. It is assumed that the output diode bridge switches ideally and requires no capacitive snubber. As stated earlier, the devices on the phase-leading pole of the input bridge are always turned-off at a lower current than those of the slaved pole. Hence, applying the minimum current constraint to the turn-off current of these devices and using the generic expression for the minimum current, eqn. (6.3.7), the minimum phase-shift, β_{min}, is evaluated as,

$$\beta_{min} = \frac{4\sqrt{d}}{\omega_n (1 + d)} + \pi d \qquad \ldots(6.5.1)$$

Substituting this expression in the average output current equation (derived for the ideal case, eqn. (3.2.13a), the influence of the input device snubber capacitance on the soft-switching region of the output voltage - output current plane can be demonstrated as shown in Fig. 6.5.1. Note, the $\omega_n = \infty$ case represents the ideal situation of no snubber capacitance. For finite snubber capacitance, for instance $\omega_n = 10$, the input bridge boundary pulls out towards the right, thus restricting the soft-switching region. A judicious design must incorporate the effects of the magnetizing inductance and snubber capacitance to optimize the soft-switching region of control and switching losses.

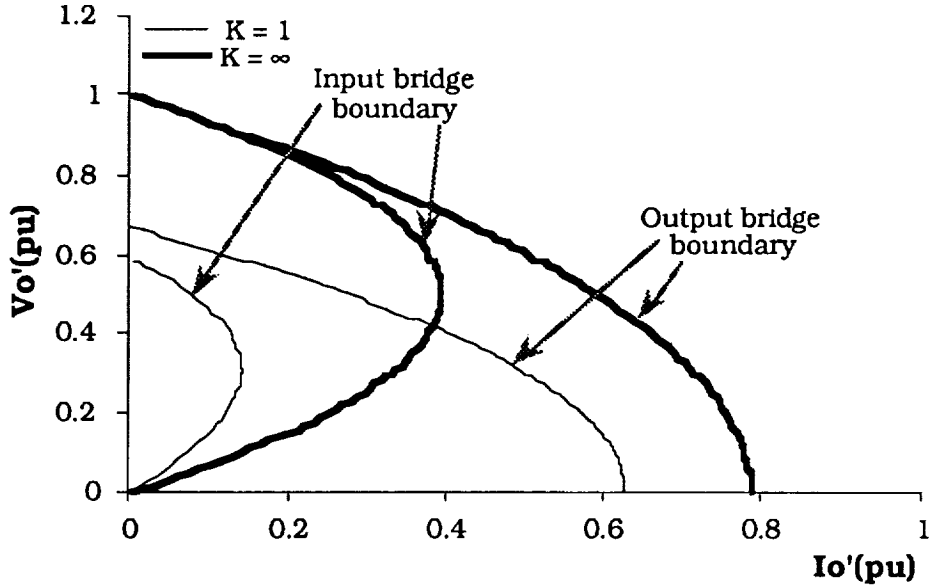


Fig. 6.5.1 Influence of magnetizing inductance on the soft-switching region on the output voltage-output current plane for Topology A. $K = L_m / L$.

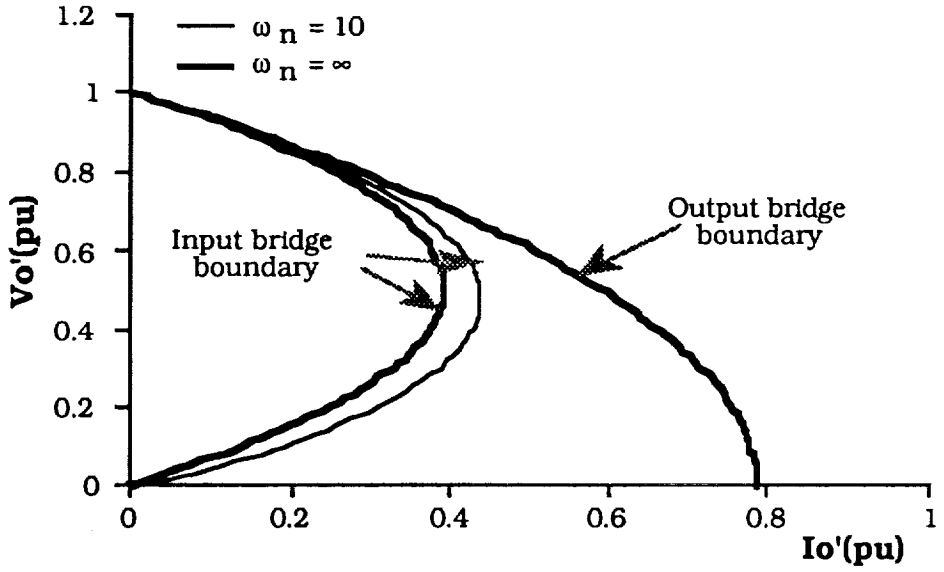


Fig. 6.5.2 Influence of snubber capacitance on the soft-switching region on the output voltage-output current plane for Topology A. ω_n decreases as snubber capacitance increases.

6.6 Summary

The influence of magnetizing inductance and snubber capacitance on the soft-switching region of operation for the two proposed single-phase converter topologies is presented. The favourable effects of reduced magnetizing inductance at lightly loaded conditions can be used to increase the very narrow region of lossless control. For both the topologies, increased snubber capacitance reduces the region of lossless operation. Hence, oversnubbing leads to the conflicting situations of reduced switching losses versus reduced region of lossless control, which must be carefully resolved.

The analysis for Topology C, although quite involved owing to the increased modes of operation, leads to observations very similar to those for Topology B.

CHAPTER 7

DESIGN CONSIDERATIONS FOR HIGH FREQUENCY TRANSFORMERS

7.1 Introduction

The transformer, a necessary element in any high power dc/dc converter for galvanic isolation, is by far the dominant factor in the power density criteria. High power density requirements of 0.2 - 0.3kg/kW with voltage outputs in the order of kilovolts coupled with the low leakage requirement, calls for a rigorous design methodology. At the very outset, the need for high operating frequencies to achieve the desired power density becomes evident.

Broadly speaking, the two fundamental issues in the design of any high-power high-frequency transformer are minimum losses and low leakage inductance. The two loss components associated with the transformer, namely core and copper losses, are strongly related to the frequency. Core loss, for a given frequency and flux density, is material dependent. Consequently, as a first step in the design process, an investigation of various high frequency core materials is essential. Copper loss in the transformer is extremely sensitive to the leakage flux distribution in the window region, which in turn is dependent on the core and winding geometry. A major focus of this

chapter is on the influence of different winding arrangements on the winding losses and leakage inductance.

As mentioned earlier, in the proposed dc/dc converter, the presence of a certain amount of leakage inductance (governed by the rated power, frequency and design point) is crucial to the operation of the converter, since it functions as the main energy transfer element from one dc voltage source to the other. On the other hand, too high a value restricts maximum power transfer. In essence, the leakage inductance needs to be carefully controlled. This design objective is a relatively difficult task to meet in conventional transformers. Coaxial windings, used primarily for very high frequency (radio frequency range) transformers, seem to offer an interesting and viable option. The latter part of this chapter addresses such winding techniques.

7.2 Core selection

The characteristics of a good core material include low specific core losses (defined as losses per unit volume or per unit mass) at high operating frequencies, high saturation flux density, high power/weight ratio, and good thermal and mechanical properties. In the light of these characteristics the three candidates investigated are : Ferrite PC40, Permalloy80 (0.5mil) and Metglas2605SC (1mil). Table 7.2.1 lists some of their salient properties.

Table 7.2.1

(Test Core Material Properties)

	Ferrite (PC40)	Permalloy-80	Metglas2605SC
Type	Ceramic	Tape-wound	Tape-wound (Amorphous)
Composition	Fe_2O_3 50% MnO 50%	Ni 80% Fe 16% Mo 4%	Fe 81% B 13.5% Si 3.5%, C 2%
Bm(T)	0.2	0.5	0.75
μ	2300	30000	50000
Ω-m	6.5	0.57	1.25
gm/cc	4.8	8.7	7.3
Shape	Wide range- E,I,U,Toroids, Pot, etc.	Toroids, Cut C-cores	Toroids, Cut C-cores

To characterize these core materials, the specific core losses were measured for different frequencies over a wide range of flux densities under square wave voltage excitation. These tests were carried out owing to the unavailability of such data for square wave excitation. A half-bridge inverter, using Power MOSFETs as switches, was fabricated to generate the square wave voltage across a 4-turn foil-wound coil mounted on the core under test. The core loss was measured by integrating the product of the voltage and current on the coil on the LeCroy 9400 digital oscilloscope. The core loss figure includes the winding losses, which were estimated to be small enough (within 1%) to be neglected without much error. Figs. 7.2.1a, b, c & d show specific core losses (measured as mW/cc) plotted as a function of the flux density on a log-log scale for the three candidate materials at 10, 25, 50 and 100 kHz respectively.

It is seen that Metglas exhibits the highest core losses for all the test frequencies over the entire range of test flux densities, and is hence not considered to be a viable core material for our application, given the high power density and high efficiency constraints. The Permalloy-80(0.5 mil) material is the most promising of the three materials for all the test frequencies. On the other hand, even though the Ferrite material has higher losses than the Permalloy-80, the former offers a wide range of core geometries. In particular, for high power, low leakage transformer designs, the shell-type of transformer built from E-E cores is the most desirable. Such core

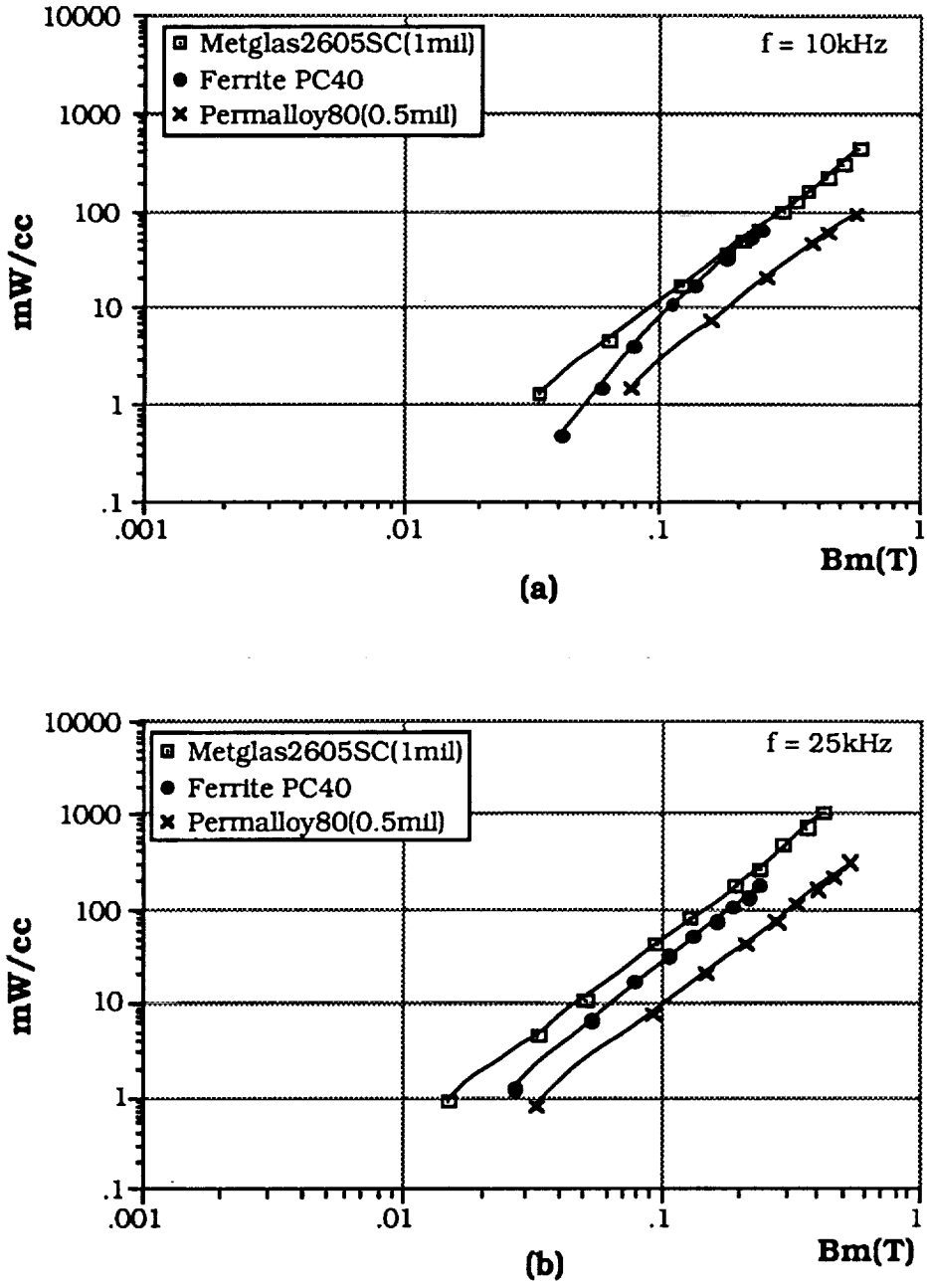
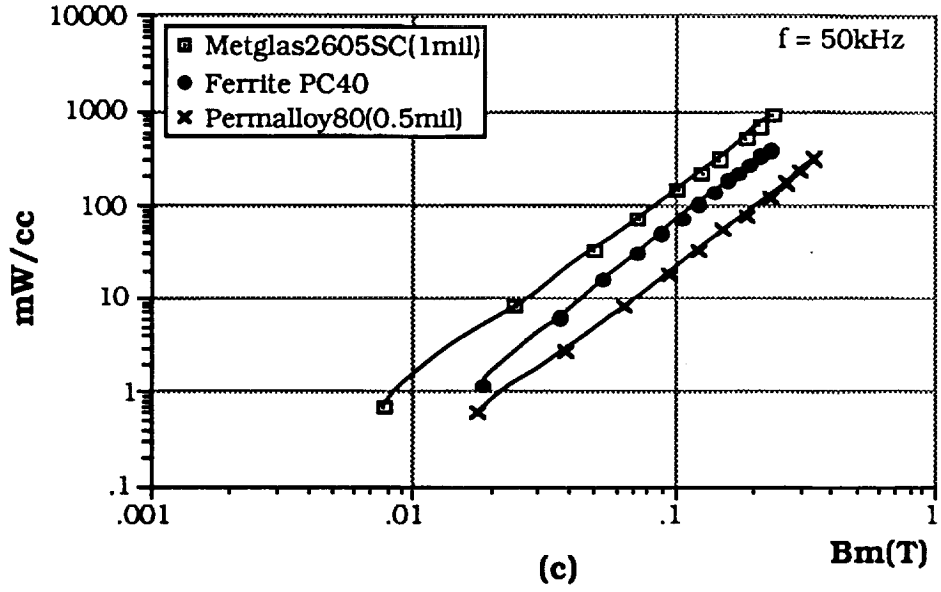


Fig. 7.2.1 Specific Core Losses (mW/cc) vs Peak Flux Density (Bm) for the three candidate materials at (a) f = 10 kHz (b) f = 25 kHz.



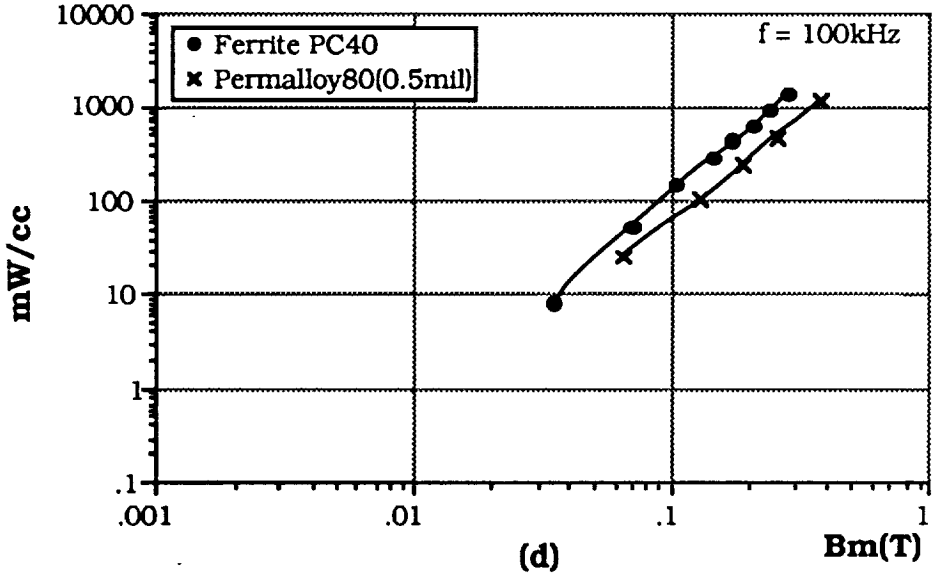


Fig. 7.2.1 Specific Core Losses (mW/cc) vs Peak Flux Density (Bm) for the three candidate materials at (c) f = 50 kHz (d) f = 100 kHz (Metglas2605SC not shown, as it is very lossy at this frequency).

shapes are readily available in the Ferrite material. Moreover, Ferrite cores are considerably cheaper than the other two core materials. In the fabrication of the final transformer for the proposed converter Ferrite cores are used for the above mentioned reasons.

The following sections outline a fairly extensive analysis of the influence of various winding parameters on the leakage flux distribution and in turn on the copper losses. Broadly speaking, this entails a study of the two possible winding arrangements - conventional and coaxial. Various interleaved arrangements of winding sections under the category of conventional windings, and two conductor geometries for the outer tubular winding under the category of coaxial windings have been investigated.

7.3 Conventional Winding Arrangements

The primary objective of this section is to study the influence of the various conventional winding geometries and parameters on the copper losses. Copper losses in a high frequency transformer are predominantly due to skin and proximity effects, which are collectively called eddy current effects.

Skin effect, associated with a conductor carrying alternating current, is the redistribution of the current towards the surface due to the magnetic field generated by this current. The resultant increase in the current density can be seen, from a circuit viewpoint,

as an increase in the effective resistance of the conductor. Consequently, for a given current the I^2R losses would increase. This phenomenon is strongly related to the frequency. Proximity effect is the phenomenon in which circulating eddy currents are induced in the conductor by time-varying magnetic fields generated from nearby current carrying conductors. These eddy currents generate extra losses and are also strongly related to the frequency and magnitude of the external field. The computation of the copper losses, accounting for eddy current effects, can be rigorously done by using finite element analysis. However, this is normally very time-consuming and gives very little physical insights into the problem. Ferreira [30] has shown, that under the assumption of a uniform magnetic field across the conductor cross-section, the current densities due to skin effect and proximity effect are spatially orthogonal to each other. Hence, the loss components due to skin and proximity effects can be independently computed.

The two losses can be expressed as,

$$P_{skin} = F * I^2 \qquad ...(7.3.1)$$

$$P_{prox} = G * H^2 \qquad ...(7.3.2)$$

where,

F is the effective resistance due to skin effect of the conductor

G is the proximity effect factor

I is the current in the conductor, and

H is the external magnetic field caused by surrounding currents.

F and G are functions of frequency, conductor type (foil, litz wire, or solid round wire), dimensions and material.

Minimization of winding losses due to the eddy current effects, in high frequency transformers is a fairly challenging task and involves, firstly, the selection of the proper conductor type and dimensions and secondly, an understanding of the influence of the winding geometry on the leakage (or, stray) field distribution in the window region. It is important to calculate this leakage field to assess the proximity effect winding losses.

To appreciate the influence of the conductor type on the effective resistance due to skin effect, for instance, three standard conductor types, viz. foil, litz wire and solid round wire are considered. For each conductor type the cross-sectional area is kept constant, to keep the dc resistance/unit length, R_{dc}, fixed. The effective resistance due to skin effect for each conductor type is given as [30,31,32],

$$F_{strip} = \frac{R_{dc}\,\gamma}{2}\left[\frac{\sinh\gamma + \sin\gamma}{\cosh\gamma - \cos\gamma}\right] \quad \Omega/m \qquad \ldots(7.3.3a)$$

where,

$$\gamma = \frac{h}{\delta}$$

$$R_{dc} = \frac{1}{h\, w\, \sigma} \quad \Omega/m$$

h = foil thickness, w = foil width

$$\delta = \text{skin depth} = \frac{1}{\sqrt{f\, \pi\, \sigma\, \mu_o}}$$

σ = electrical conductivity, μ_o = absolute permeability

f = frequency

$$F_{round} = \frac{R_{dc}\, \gamma}{2}\left[\frac{ber(\gamma)\, bei'(\gamma) - bei(\gamma)\, ber'(\gamma)}{ber'^2(\gamma) + bei'^2(\gamma)}\right] \quad \Omega/m$$

...(7.3.3b)

where,

ber(.), bei(.) and bei'(.) are the Kelvin functions,

$$\gamma = \frac{d}{\delta\sqrt{2}}$$

$$R_{dc} = \frac{4}{\pi\, \sigma\, d^2} \quad \Omega/m$$

d = diameter of round wire

$$F_{litz} = \frac{F_{strand}}{N} = \frac{N\, R_{dc}\, \gamma}{2}\left[\frac{ber(\gamma)\, bei'(\gamma) - bei(\gamma)\, ber'(\gamma)}{ber'^2(\gamma) + bei'^2(\gamma)}\right] \quad \Omega/m$$

...(7.3.3c)

where,

$$\gamma = \frac{d_{strand}}{\delta\sqrt{2}}$$

$$R_{dc} = \frac{4}{\pi\, \sigma\, N\, d_{strand}^2} \quad \Omega/m$$

d_{strand} = litz strand diameter (enamel thickness neglected)

N = number of litz strands

A standard litz wire is selected, consisting of 329 strands and a total cross-sectional area of 16585cmils (1 cmil = $\pi/4$mil^2, where, 1 mil = 25.4 * 10^{-6} m). Keeping this as the common cross-sectional area, and choosing f = 50 kHz, the effective resistance for each conductor type, as given by eqns. (7.3.3a, b, c), is computed. The thickness of the foil is selected as 2δ, where $\delta \sim$ 12mils at f = 50 kHz (for copper). Table 7.3.2 summarizes the effective resistance for each conductor type based on the above considerations. As expected the solid round conductor shows the highest increase in effective resistance, and is certainly not suitable as a conductor type for high frequency applications. Foil and litz wire show very little change in their effective resistances from the dc value. Of course, as foil

thickness is increased its effective resistance goes up. The choice between the two conductor types, for high frequency transformer applications, is thus dependent on various design trade-offs including relative window dimensions, window fill factor, number of turns, etc.

As a first consideration, the choice of core geometry is dictated by the low leakage inductance desired, and also, the winding arrangement. The use of shell-type core for conventional transformers, made from E-E cores, is seen to be desirable. This, in turn, leaves us with Ferrite as the core material of choice (for reasons mentioned in the last section). Other attractive geometries such as pot-cores, are not available for the high power levels of interest.

To address the issue of the influence of winding geometry on leakage flux distribution, three typical conventional winding arrangements, labelled X, Y and Z, shown in Fig. 7.3.1 are studied. Arrangement X consists of one primary and one secondary winding wound concentrically on the centerpost of a shell-core. Arrangement Y consists of one secondary winding sandwiched between two primary windings, which are connected in parallel. All the winding sections are wound concentric to the centerpost. Arrangement Z consists of the same winding sections as in Y, with the sections now stacked vertically, concentric to the centerpost. The two primary sections are connected in parallel. To analyze the copper losses, the transformer for each winding arrangement is designed for the actual

Table 7.3.2

(Eff. Resistance due to Skin Effect for the three conductor types)

(f = 50 kHz, δ ~ 12 mils)

	Rdc (Ω/m)	F (Ω/m)	% Change
Foil (h = 2δ)	2.0229	2.2571	11.6 %
Solid Round	2.0229	6.1756	205.3 %
Litz wire (329 strands)	2.0229	2.0223	0.02 %

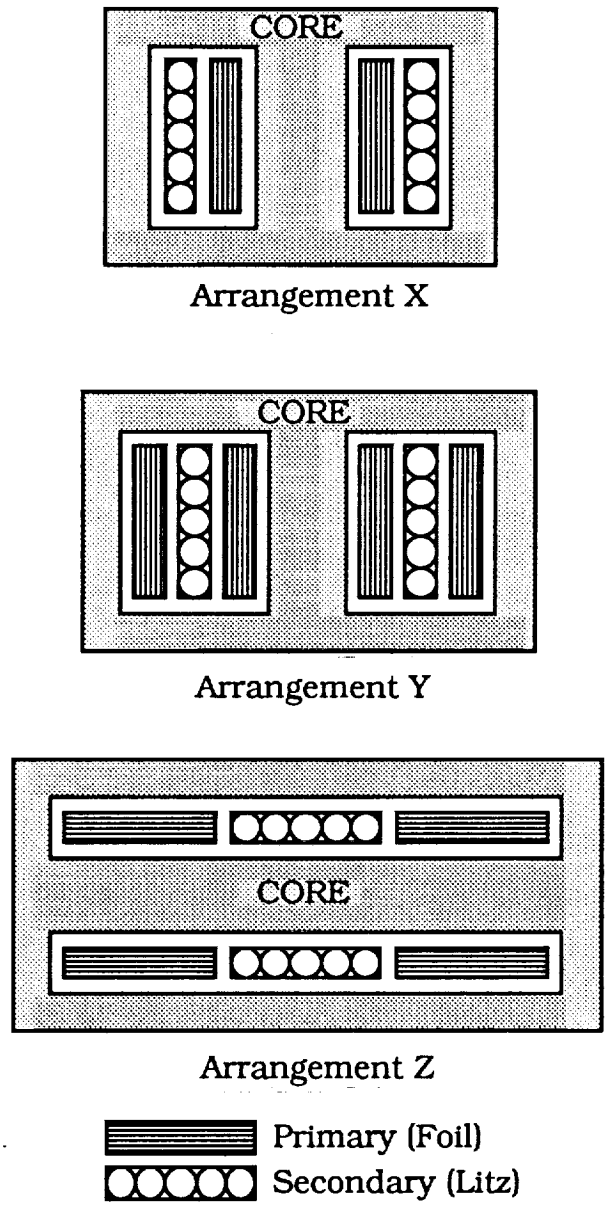


Fig. 7.3.1 Schematics of three conventional transformer winding arrangements X, Y, Z.

specifications, viz, 50 kW, 50 kHz, 200 Vpk (square wave) primary and 2000 Vpk (square wave) secondary, maintaining the same amount of copper. Due to the unavailability of a finite element eddy current solver package at our computing facility at the present time, the computation of these losses was done with the aid of a high frequency transformer design program [30].

This software referred to as "TID" by its author takes as inputs pertinent core, window and winding section dimensions. It also accounts for the conductor type (foil, litz wire or round) with all its relevant dimensions. The Fourier components of the current flowing in each winding must also be specified. It then computes the total winding losses by calculating the skin effect and proximity effect losses separately (noting, their orthogonal relationship under the assumption of a uniform field) for each frequency component and simply adding all the terms together. The loss due to skin effect is computed as given in eqn. (7.3.1). As seen from the proximity effect eqn. (7.3.2), the field distribution in the window region must first be calculated. This is done using the method of images, which in essence consists of replacing the effects of a boundary on an applied field by simple distributions of currents behind the boundary line, the desired field being given by the sum of the applied and the image fields [33].

Setting the maximum operating flux density at 0.2T, typical for the selected Ferrite material, the required core cross-sectional area is calculated from the transformer voltage relation given below,

$$V_{primary} = 4 * N_{primary} * B_{max} * f * A_c \qquad ...(7.3.4)$$

where, $N_{primary}$ is the number of primary turns, f is the frequency of operation and A_c is the core cross-sectional area. Note, since the excitation voltage is square-wave, the form factor is 4. At this point, however, the number of primary turns is also not known. Considering the high levels of primary current and the high turns ratio required, $N_{primary}$ is set to 3. Moreover, to maintain a reasonably high fill factor, and given the constraint of providing sufficient insulation at the high voltage levels, a foil-type of primary conductor is selected. The core cross-sectional area can now be determined from eqn. (7.3.4), and further the core centerpost dimensions is ascertained.

The primary foil thickness is chosen to be 2δ, where δ is the skin-depth (at 50 kHz). The conductor type for the secondary winding, consisting of 15 turns, is selected as litz wire. To determine the amount of copper area, the current density and operating r.m.s. current at full power must be known. A typical choice for the current density at such power and size levels is 500 c.mil/A. To ascertain the rated current, a reasonable design point is

selected from the transformer kVA versus output power characteristics for Topology B, shown in Fig. 7.3.2. On the d = 1 (corresponding to the input voltage being equal to the primary-referred output voltage) curve, the design point is chosen so that the transformer utilization, defined as the ratio of output power to transformer kVA, is fairly high. Note also that the d=1 is a good design choice because the transformer utilization is fairly constant over a wide range of phase-shift. The normalized output power for Topology B is given as,

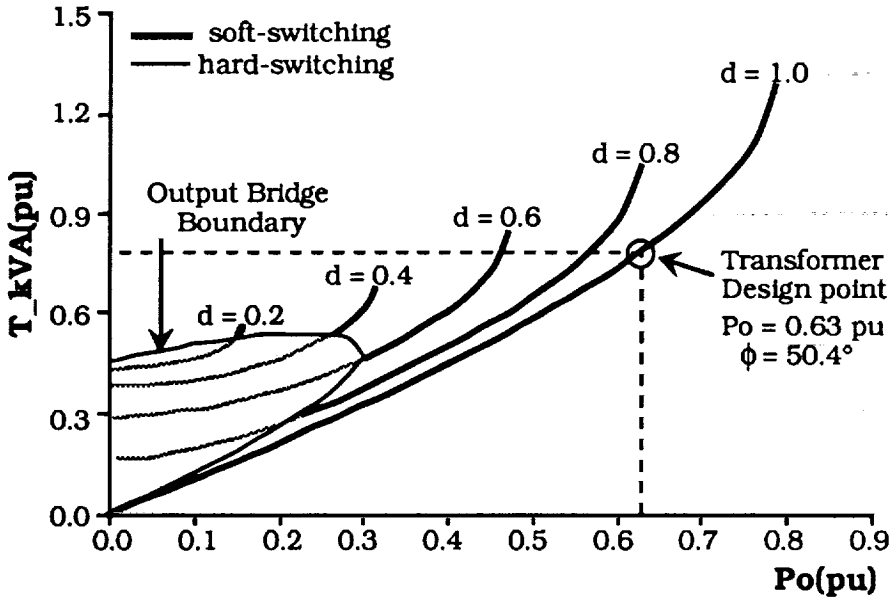


Fig. 7.3.2 Transformer-kVA versus output power for Topology B, showing the selected transformer design point.

$$P_o(pu) = d\,\phi\,(1 - \frac{\phi}{\pi}) \qquad ...(\ 7.3.5\ )$$

where, d is the dc conversion ratio, referred to the primary side, and ϕ is the controlled phase-shift between the the input and output bridges. The selected design point corresponds to P_o = 0.63 pu (normalized). Substituting this in eqn. (7.3.5) and setting d = 1, gives ϕ = 50.4°. Now, the normalized selected design point must correspond to the rated output power of 50 kW. The power base is given as,

$$P_b = \frac{V_i^2}{\omega L}$$

Hence,

$$0.63 * P_b = 50 \text{ kW}$$

Substituting V_i = 200V and $\omega = 2\pi f$, we arrive at,

$$L = 1.6\ \mu H$$

where, L is the required transformer leakage inductance at f = 50kHz.

Further, knowing ϕ, d, L, f and V_i, the primary rated r.m.s. current is 312 A, while the secondary rated rms current is 31.2 A. Knowing the rated current levels in each winding and the specified current density, the primary foil dimensions are completely defined. For the secondary litz wire, an equivalent AWG of 6 is needed. Next,

as required by the "TID" program the winding and window dimensions, and the Fourier series component of the primary and secondary current at the design point are calculated. Appendix C gives the Fourier series analysis of the transformer current under ideal conditions. From this analysis, the dominant harmonic components at the design point, are computed as,

Primary current components:

I_1 = 430.3 Apk; I_3 = 109.2 Apk; I_5 = 32.7 Apk;

Secondary current components:

I_1 = 86.1 Apk; I_3 = 21.8 Apk; I_5 = 6.5 Apk;

Table 7.3.3 summarizes the copper losses, computed by the program, for each of the three arrangements - X, Y, Z. As a demonstration, Appendix D shows all the details required by the program, "TID", for arrangement Y. It is seen that the arrangement Y is the best, in terms of incurring least copper losses. The reduction in copper losses from arrangement X to Y can be explained as follows. A split up of the primary winding into two sections in Y, results in a peak field intensity half of that of X, in the window region. The ampere-turn waveform in the window region for the two winding arrangements is shown in Fig. 7.3.3 to give an idea of the relative peak field intensities. Since, the proximity effect losses are

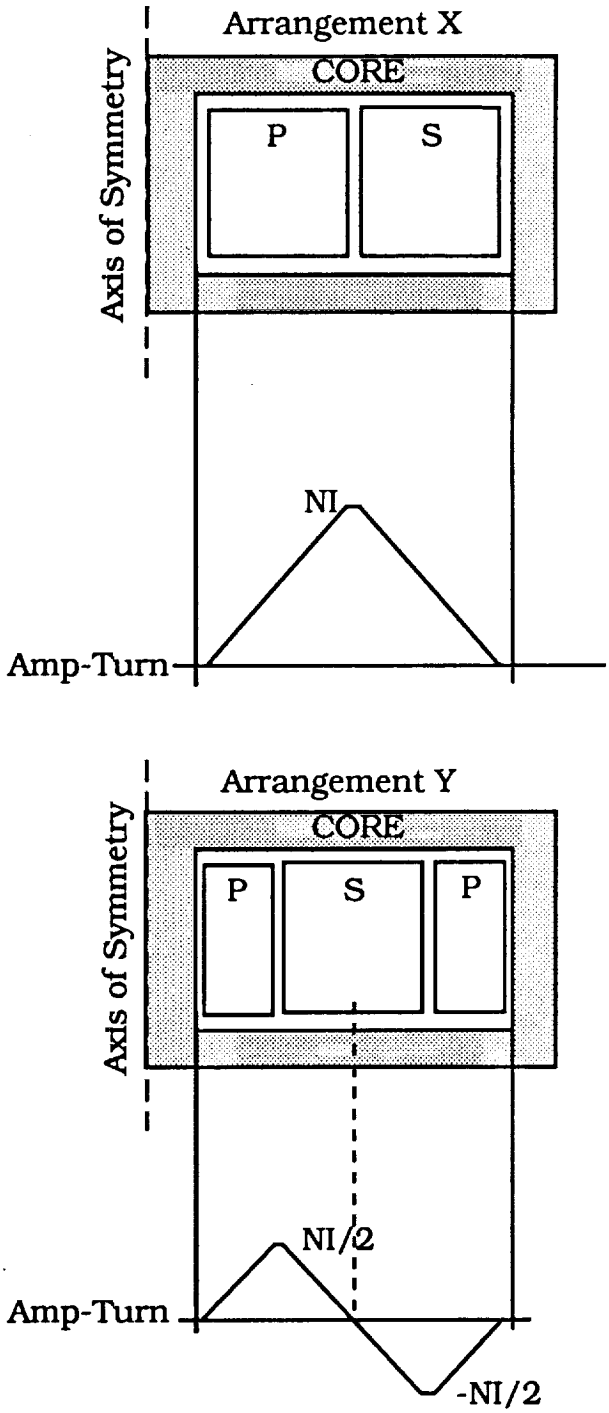


Fig. 7.3.3 Ideal ampere-turn waveforms in the window region for winding arrangements X and Y.

proportional to the square of the leakage field, arrangement Y experiences lower proximity effect losses as compared to that of X. However, this does not explain the increased losses in arrangement Z, which is simply a different permutation of Y. To understand this a flux distribution of the three arrangements was generated using a magnetostatic finite element solver [ANSOFT package]. Fig. 7.3.4 depicts the flux distribution for each arrangement in the absence of eddy currents. Recalling that the primary windings are foil-wound, in arrangement Z it is seen that the flux lines enter the primary foil-plane perpendicularly. Eddy currents are readily induced in the foil-plane, since a large surface area is available for conduction. These eddy currents, as a result of the pronounced proximity effect, give rise to the very large copper losses observed in Table 7.3.3.

In short, to minimize copper losses, windings must be sectionalized and interleaved to reduce field intensities in the window region. Moreover, these sections must also be arranged such that the flux lines are directed parallel to foil planes.

As seen from the flux plots for the conventional windings, a considerable amount of leakage flux gets coupled into the core. In designs where the leakage flux is small, it may not be very important. However, for converters where the leakage inductance is the main power transfer element, this could contribute substantially to localized saturation of the core, resulting in local hot spots and additional core losses. A preferred technique is the use of coaxially

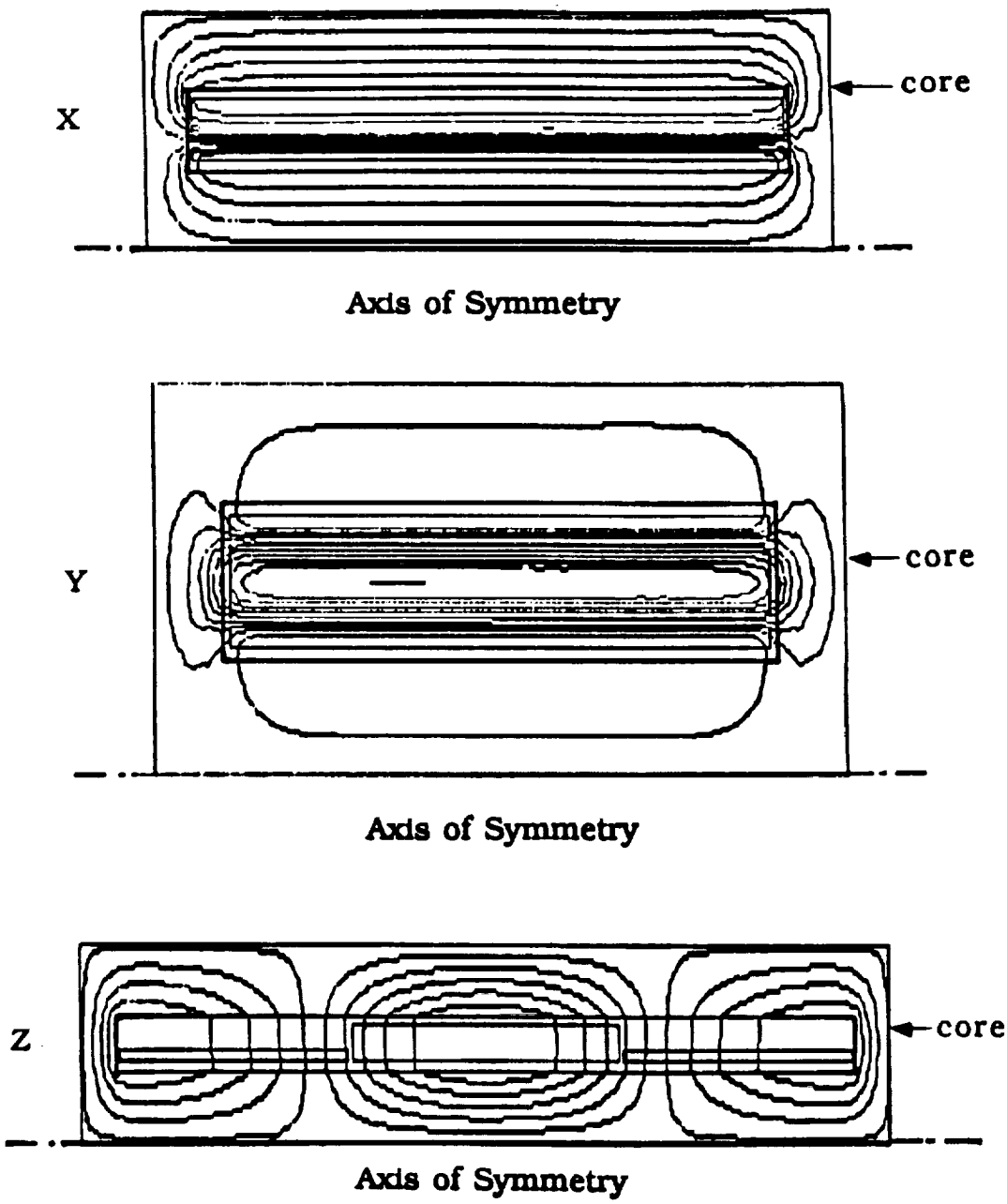


Fig. 7.3.4 Leakage flux plots for the three conventional winding arrangements, in the absence of eddy currents.

Table 7.3.3

(Summary of winding losses in the three arrangements)

(P_O = 50kW, V_i = 200Vdc, V_O=2000Vdc, f = 50kHz)

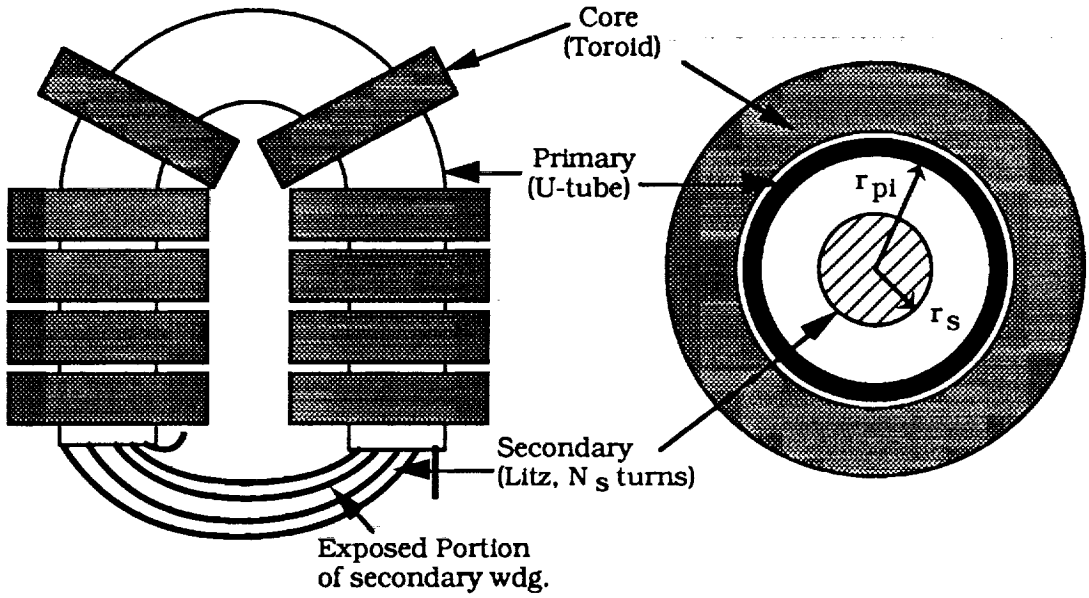
	X	Y	Z
Primary (W)	179	144	301
Secondary (W)	97	32	297
Total (W)	276	176	598

wound transformers, a well-known technology in the area of radio frequency magnetic component design.

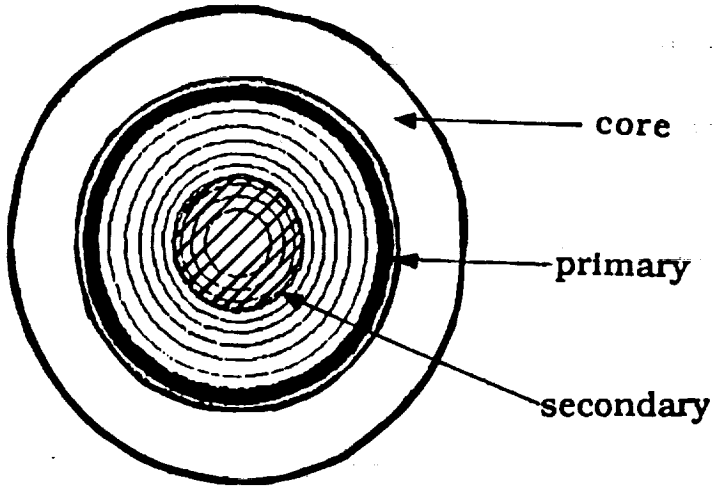
7.4 Coaxial Winding Arrangements

Fig. 7.4.1a shows a coaxially wound transformer using tubular conductors of circular cross-section, the simplest possible geometry for such transformers. The primary consists of a single turn made from a U-shaped tube of circular cross-section. The thickness of the tube must be maintained within a skin-depth (12 mils at 50 kHz). However, from the standpoint of mechanical rigidity the thickness of the tube should be at least 2 to 3 times this value. The inner secondary winding is of litz wire. The preferred core geometry is toroidal. Multiple toroidal cores can be slipped on the primary winding, depending upon the core area desired.

A point worth mentioning here is with regard to the choice of core material. As far as conventionally wound transformers are concerned, it is seen that the optimum choice of core geometry is the shell-type built from E-E cores, for high power applications. This leaves us with Ferrite as the material of choice, given the unavailability of such shapes in the Permalloy-80 tape-wound material for single-phase applications. On the other hand, for coaxial transformers with circular cross-section, a toroid is the optimum core geometry. Also, from a standpoint of fabrication, at higher



(a)



(b)

Fig. 7.4.1 (a) Coaxially wound transformer with primary tube of circular cross-section. (b) Leakage flux distribution.

power levels the number of turns on the outer tubular winding gets limited to one. This would drastically lower the magnetizing inductance if Ferrite is used as the core material, for a given core cross-section. The much higher permeability of Permalloy-80 tape-wound cores and their availability in toroidal shapes, does suggest their suitability for coaxial transformers.

A flux plot for the above arrangement, under loaded conditions, is shown in Fig. 7.4.1b. This is obtained using the magnetostatic finite element analysis software [ANSOFT]. As expected, the leakage flux is uniformly confined to the region inside the outer tube only. This is the flux due to the inner secondary winding. As mentioned earlier, this is certainly very desirable since the core is free from the effects of any localized saturation.

The leakage flux consists of the internal flux of the secondary winding and the flux within the interwinding space, which is linked by the secondary winding only. Hence, the leakage inductance per unit length can easily be derived as,

$$L_{cir} = \frac{N_s^2 \mu_o}{4\pi}\left[\frac{1}{2} + \ln\left(\frac{r_{pi}}{r_s}\right)\right] \text{ H/m} \qquad \ldots(\ 7.4.1\ )$$

where, r_{pi} is the inner radius of the primary tube (outer conductor), and r_s is the radius of the composite secondary winding, and N_s is the number of secondary turns. It is seen from eqn. (7.4.1) that for a

given N_S as the interwinding space is reduced by decreasing r_{pi}, the leakage inductance decreases. This is the most interesting feature of the coaxial winding, in that the leakage inductance is so easily controllable. In the above expression it is assumed that the inner winding is completely enclosed by the outer tubular winding. However, as shown in Fig. 7.4.1a, this is not true. The portion of the inner winding that is not enclosed, simply contributes to the leakage inductance. If a high leakage inductance is desired, and the interwinding space is at a premium, then the length of the exposed inner winding can be judiciously controlled to achieve the objective.

The transformer is also mechanically very robust. The electromechanical forces on the windings, which could potentially be large enough to damage the transformer core at the high current levels expected, are lower than for conventional designs, as the leakage flux can be controlled and confined within the outer conductor.

Another coaxial winding geometry that is under investigation uses a primary conductor of rectangular cross-section. This facilitates the use of E-E cores, if Ferrites is the core material of choice. Fig. 7.4.2a shows the top view of such a coaxial winding. Fig. 7.4.2b shows its leakage flux distribution obtained from the magnetostatic finite element analysis, which assumes uniform current distribution. Under such conditions considerable amount of

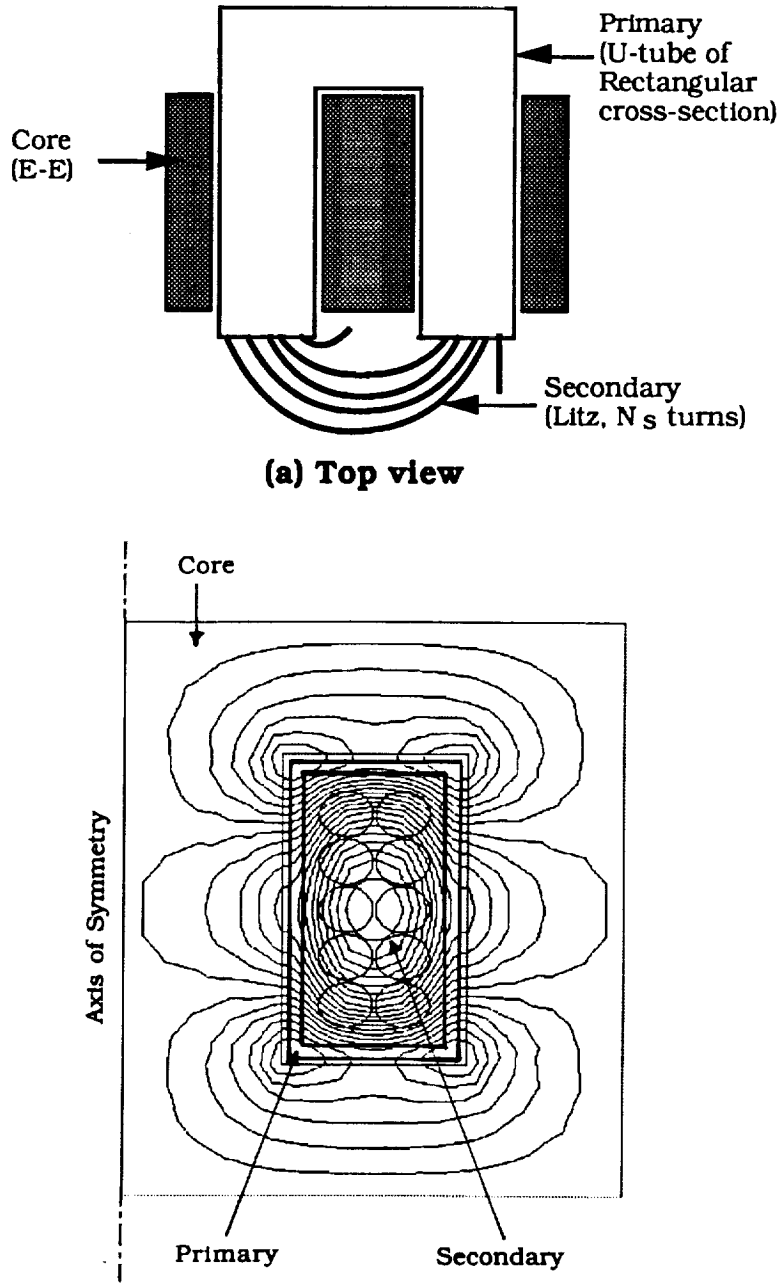


Fig. 7.4.2 (a) Coaxially wound transformer with primary tube of rectangular cross-section. (b) Leakage flux distribution around one tube of the primary.

leakage flux would permeate the core, in particular at the corners of the tube, as seen from the flux plot. This is so, because of the asymmetry in the winding in the radial direction. However, in reality, the leakage fluxes entering or leaving the tube induce eddy currents, which by Lenz's law would tend to oppose this leakage field. The resultant effect is a redistribution of the current in the outer tube with the current densities highest near the central portion of each side. From intuition the majority of the resultant leakage field would still stay confined within the outer tube. This proposition remains to be verified from an eddy current finite element analysis. Compared to the circular coaxial winding, an equivalent rectangular coaxial would incur higher copper losses because of the eddy currents induced as discussed above. Also, in the rectangular coaxial winding, the core sees some leakage flux, particularly at the corners.

The two geometries of coaxially wound transformers discussed above were designed and fabricated for the converter specifications, and the results are presented in the following section.

7.5 Test Results from Coaxially Wound Transformers

7.5.1 Rectangular Coaxial Geometry

Fig. 7.5.1 shows the schematic of a vertical cross-section of the transformer fabricated in the laboratory. Fundamentally, the

transformer construction is that of the standard shell-type. Two secondary windings are wound inside a copper tube of rectangular cross-section. Fig. 7.5.2 is a photograph of the prototype transformer. The constructional details of the transformer are listed in Table 7.5.1. The open circuit and short circuit measurements at 50 kHz are shown in Fig. 7.5.3. Table 7.5.2 summarizes the rated losses, projected kVA, power density and efficiency, and measured parameters.

7.5.2 Circular Coaxial Geometry

Fig. 7.5.4 is the schematic of a vertical cross-section of the transformer fabricated in the laboratory. As stated earlier, although Permalloy-80 is a desirable candidate for such a geometry because of its higher permeability, lower specific core losses at 50 kHz and availability in toroidal shapes, the core material used in the prototype is Ferrite primarily for cost reasons. Fig. 7.5.5 is a photograph of the prototype transformer. The constructional details of the transformer are listed in Table 7.5.3. The open-circuit and short-circuit measurements at 50 kHz are shown in Fig. 7.5.6. Table 7.5.4 summarizes the rated losses, projected kVA, power density and efficiency, and measured parameters.

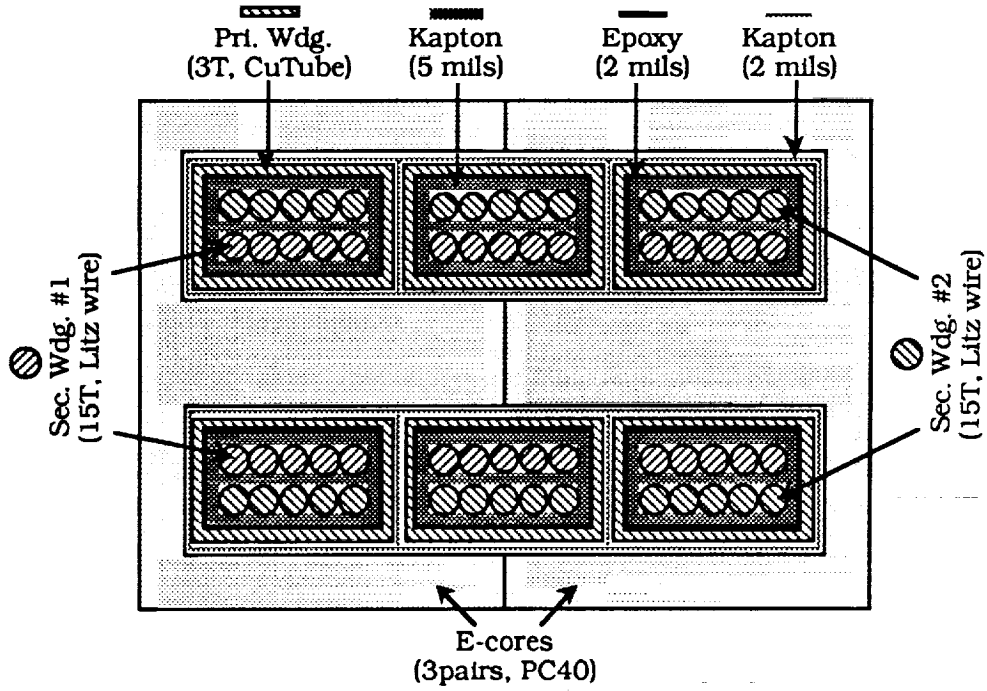


Fig. 7.5.1 Schematic of the vertical cross-section of the fabricated 50 kVA, 50 kHz rectangular coaxial transformer. Dimensions not to scale.

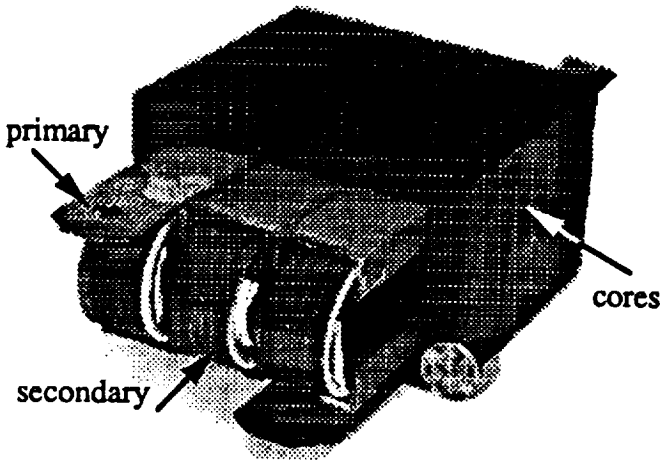


Fig. 7.5.2 Scanned photograph of the prototype 50 kVA, 50 kHz rectangular coaxial transformer. The constructional details are given in Table 7.5.1.

Table 7.5.1

(Constructional details of Rectangular Coaxial Transformer)

Core:

Material: Ferrite PC40 (manufacturer : TDK, Part No. EI70)

Shape: E-E, 3 pairs

Core Area: 2.125×10^{-6} m^2

Core Volume: 502.7×10^{-6} m^3

Bmax: 0.15 T

Weight: 2.413 kg

Windings:

Primary: 1 winding

Conductor Type: Copper Rectangular tube

No. of turns: 3

Wall thickness: 1000 μm = 3δ, δ=305 μm is skin depth at 50 kHz

Current density: 4.46×10^6 A/m^2

Secondary: 2 windings

Conductor Type: Litz wire, AWG 10, 660 strands, 5x3/44/38

No. of turns: 15 each

Current density: 5.83×10^6 A/m^2 (≈ 340 c.mil / A)

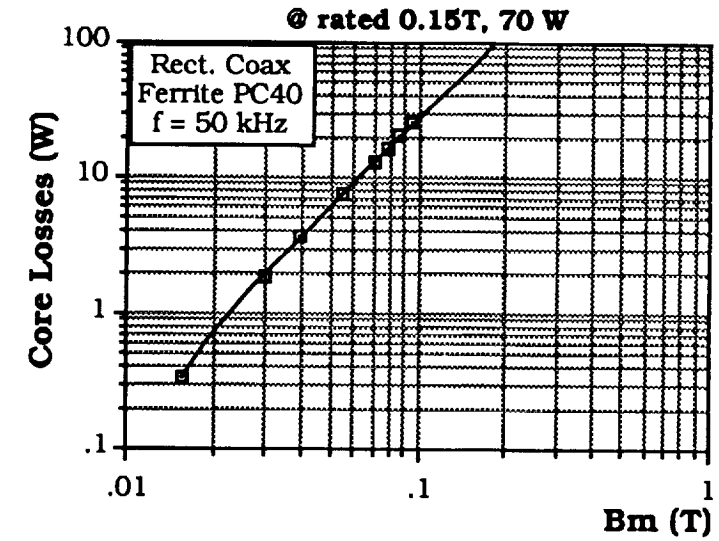
Insulation:

Epoxy: Inside walls of primary tube

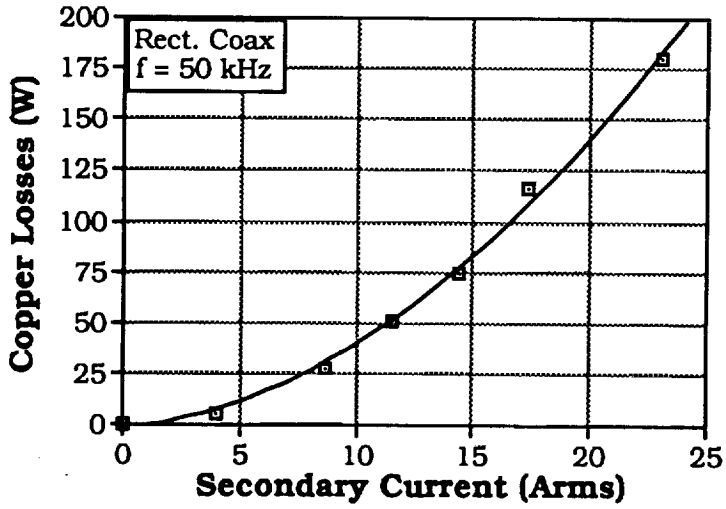
Kapton: Between secondary windings, 5 mils (1mil=25.4 μm)

Window Fill Factor: 40%

Total Weight: 3.834 kg



(a)



(b)

Fig. 7.5.3 (a) Open circuit (core loss), and (b) Short circuit (copper loss) measurements on the prototype 50 kVA, 50 kHz rectangular coaxial transformer. Results are summarized in Table 7.5.2.

Table 7.5.2
(Test Results of Rectangular Coaxial Transformer)

Magnetizing Inductance (primary referred) = 250 μH

Leakage Inductance (primary referred) = 150 nH

DC Resistance of Primary Winding = 0.289 mΩ

DC Resistance of Secondary Winding # 1 = 22.17 mΩ

DC Resistance of Secondary Winding # 2 = 23.57 mΩ

Core Losses = 70W @ 200Vrms (primary), 0.15T, 50 kHz

Copper Losses = 180W @ 230Arms on primary (limited thermally)

Projected kVA = 200 Vrms * 230 Arms = 46 kVA

Total Losses = 250W @ Projected kVA

Projected Efficiency (@ 46 kVA) = 99.4 %

Projected Power Density (@ 46 kVA) = 0.083 kg/kW

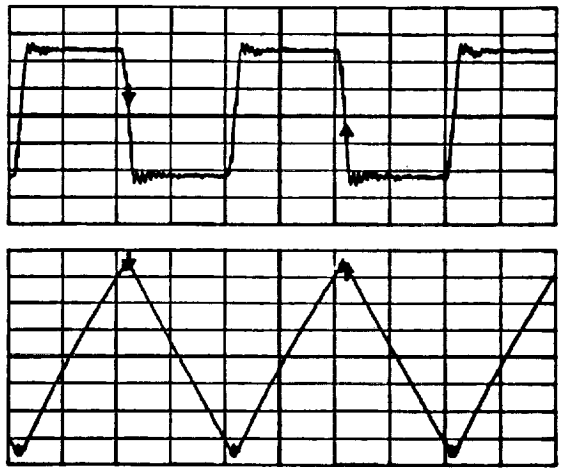


Fig. 7.5.3 (c) Oscillograms under short circuit conditions, for the prototype 50 kVA, 50 kHz rectangular coaxial transformer. Top trace : Secondary voltage, 50 V/div ; Bottom trace : Primary current, 100 A/div, Time : 5μs/div.

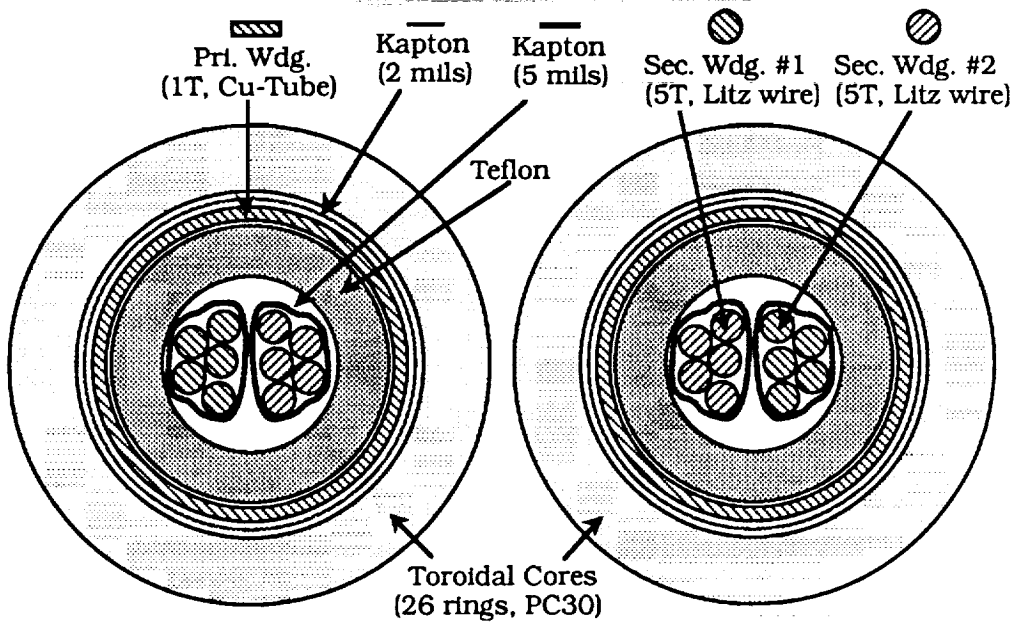


Fig. 7.5.4 Schematic of the vertical cross-section of the fabricated 50kVA, 50kHz circular coaxial transformer. Dimensions not to scale.

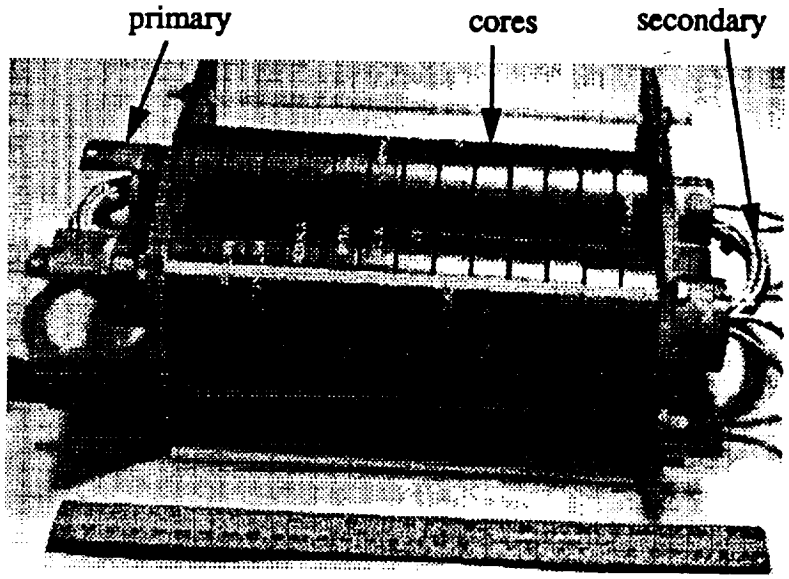


Fig. 7.5.5 Scanned photograph of the prototype 50kVA, 50kHz circular coaxial transformer. The constructional details are given in Table 7.5.3.

Table 7.5.3

(Constructional details of Circular Coaxial Transformer)

Core:

Material: Ferrite PC30 (manufacturer : TDK, T68 x 16.5 x 44)

Shape: Toroid, 26 pieces

Core Area: 5.148×10^{-3} m^2

Core Volume: 906×10^{-6} m^3

Bmax: 0.15 T

Weight: 4.368 kg

Windings:

Primary Winding: 1 winding

Conductor Type: Copper Circular tube

No. of turns: 1

Wall thickness: 1000 μm = 3δ, δ=305 μm is skin depth at 50 kHz

Current density: 1.90×10^6 A/m^2

Secondary Windings: 2 windings

Conductor Type: Litz wire, AWG 10, 660 strands, 5x3/44/38

No. of turns: 5 each

Current density: 5.83×10^6 A/m^2 (≈ 340 c.mil / A)

Insulation:

Teflon: Inside walls of primary tube

Kapton: Between secondary windings, 5 mils (1mil=25.4 μm)

Window Fill Factor: 15% (intentionally low for higher leakage inductance)

Total Weight: 6.25 kg

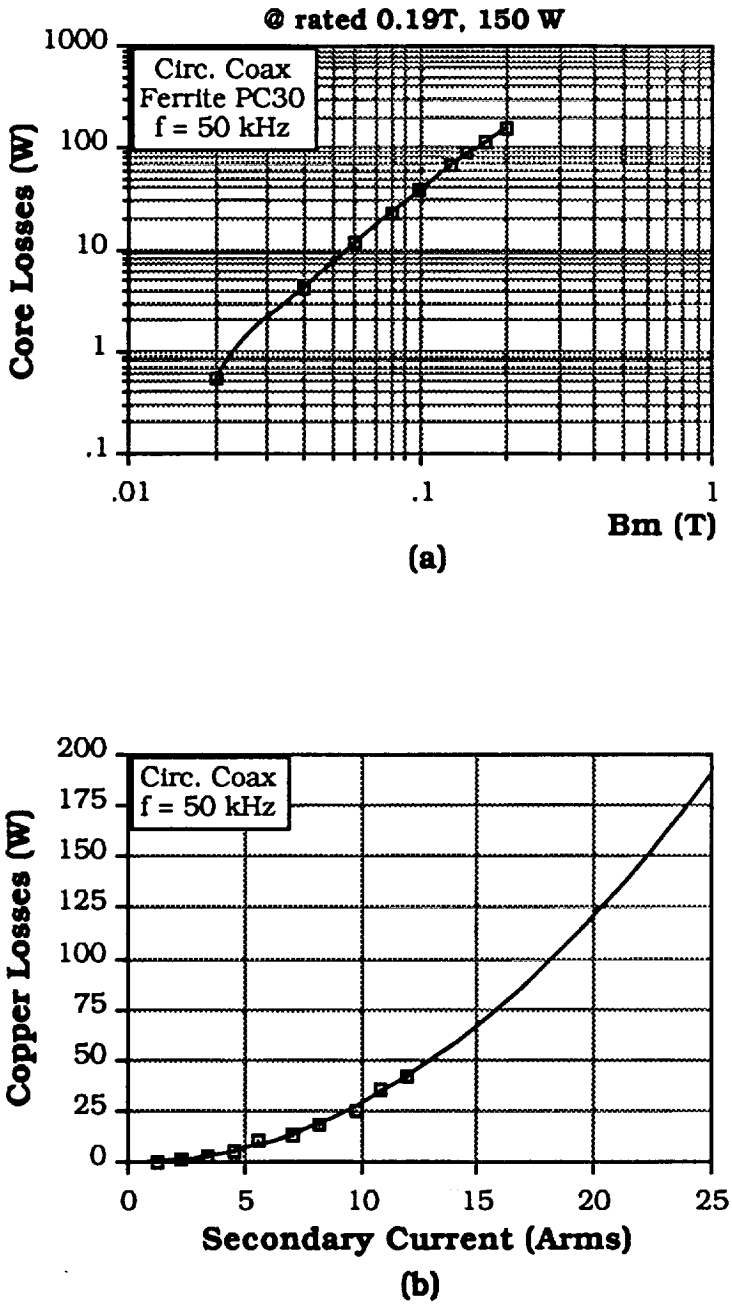


Fig. 7.5.6 (a) Open circuit (core loss), and (b) Short circuit (copper loss) measurements on the prototype 50 kVA, 50 kHz circular coaxial transformer. Results are summarized in Table 7.5.4.

Table 7.5.4

(Test Results of Circular Coaxial Transformer)

Magnetizing Inductance (primary referred) = 120 μH

Leakage Inductance (primary referred)

Measured = 250 nH

Calculated = 182 nH (from eqn. 7.4.1)

DC Resistance of Primary Winding = 0.076 mΩ

DC Resistance of Secondary Winding # 1, 2 = 23.7 mΩ

Shunt Capacitance (primary side) = 1 nF

Core Losses = 150W @ 200Vrms (primary), 0.19T, 50 kHz

Copper Losses = 190W @ 250Arms on primary (limited thermally)

Projected kVA = 200 Vrms * 250 Arms = 50 kVA

Total Losses = 340W @ Projected kVA

Projected Efficiency (@ 50 kVA) = 99.3 %

Projected Power Density (@ 50 kVA) = 0.125 kg/kW

7.6 Three-phase Coaxially Wound Transformers

The major advantage of Topology C is the much lower kVA rating of the input and output filter capacitors. This indeed could be an important consideration for high power density converters. However, it is crucial that the leakage inductance, which is the main energy transfer element, be almost identical in each phase of the transformer to ensure balanced operation. This requires that the transformer be physically symmetrical. A possible geometry, with symmetrical core structure, is discussed in Appendix A. However, the unavailability of suitable core shapes, especially in high frequency materials, would render the construction of such a transformer rather challenging.

Again, coaxial winding techniques offer a viable solution to the construction of such 3-phase transformers [34]. Fig. 7.6.1 shows a schematic of a coaxially wound Y-Y transformer. The primary of each phase consists of a straight tube of circular cross section. The star point is realized by shorting the tubes at one end. Toroidal cores are slipped over each tube to form the magnetic medium. The secondary wire can now be wound inside the primary tube. Only one turn on the secondary is shown. In essence, this construction is simply three 1-phase transformers connected to form the 3-phase transformer. Although, the structure is completely symmetrical, it suffers from the problem of being unable to drive a single phase load. This can be demonstrated by the following simple analysis.

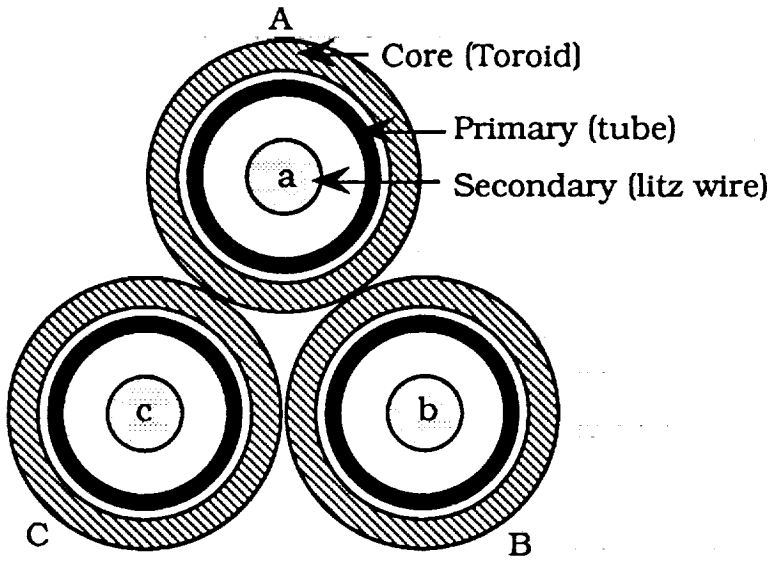


Fig. 7.6.1 Schematic of a 3-phase coaxially wound Y-Y transformer

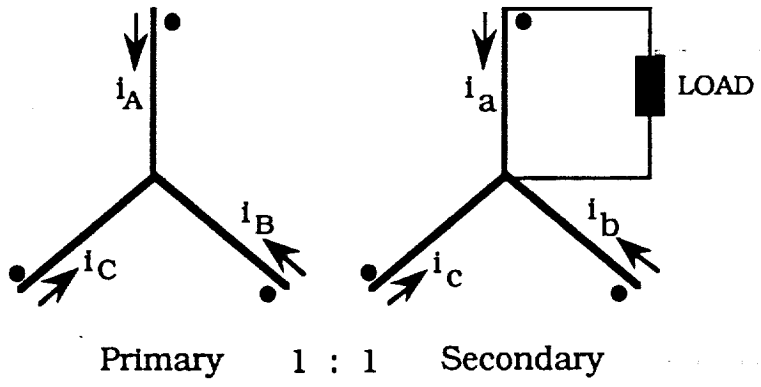


Fig. 7.6.2 Circuit schematic of the 3-phase coaxially wound Y-Y transformer, with secondary phase 'a' loaded.

Assume the transformer is ideal in that it has zero leakage inductance and infinite magnetizing inductance. Let the secondary consist of 1 turn (the primary must have 1 turn only). Fig. 7.6.2 shows the circuit diagram of the 3ϕ Y-Y transformer with secondary phase 'a' loaded. Applying ampere-turn balance, (note, primary variables are denoted with capital subscripts and secondary variables with small subscripts)

$$i_A = - i_a, \qquad i_B = - i_b, \qquad i_C = - i_c.$$

Now,

$$i_b = 0 = i_c$$

Hence,

$$i_B = 0 = i_C$$

But,

$$i_A + i_B + i_C = 0$$

Hence,

$$i_A = 0$$

which implies,

$$i_a = 0$$

This is only possible if the voltage on secondary phase 'a' collapses. Note, the underlying reason for such a behaviour is that no magnetic coupling exists between the phases. To overcome this

problem, the secondary can be wound in a "zig-zag" fashion, shown schematically in Fig. 7.6.3. All the secondary windings have the same number of turns. Repeating the above mode of analysis for single phase loading, we get

$$i_A + i_a - i_b = 0$$

$$i_B + i_b - i_c = 0$$

$$i_C + i_c - i_a = 0$$

But,

$$i_b = 0 = i_c$$

Hence,

$$i_A = -i_a, \quad i_B = 0, \quad i_C = i_a$$

Thus, it is seen that such a connection allows single phase loading. Fig. 7.6.4 shows a cross-sectional view of the 3ϕ coaxially wound transformer, with the secondary connected in a "zig-zag" manner.

7.7 Summary

Various design considerations on high-power, high-frequency transformers are investigated. Core loss characteristics for three high frequency materials are presented. Although, Ferrite (PC40) is lossier than Permalloy-80 (0.5 mil), at the frequencies of interest (25 - 50 kHz), the use of the former is justified on the basis of cost,

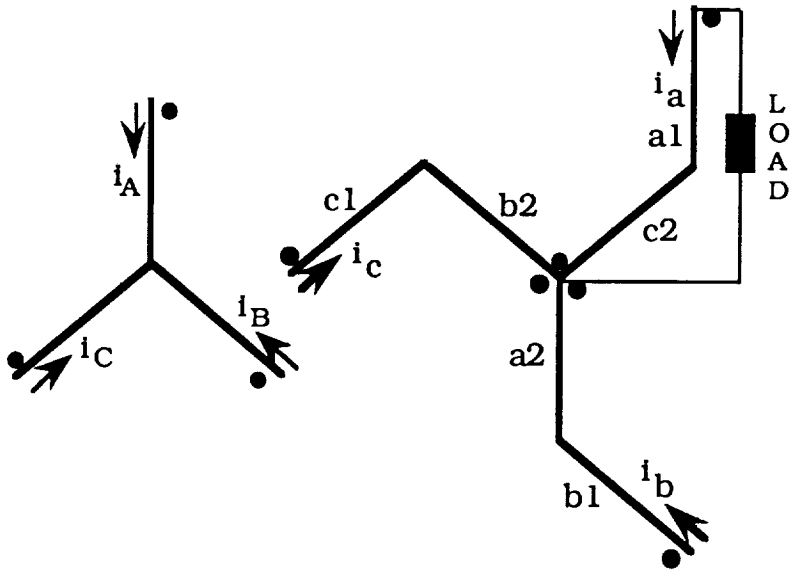


Fig. 7.6.3 Circuit schematic of a 3-phase coaxially wound Y-Y transformer, with "zig-zag" secondary.

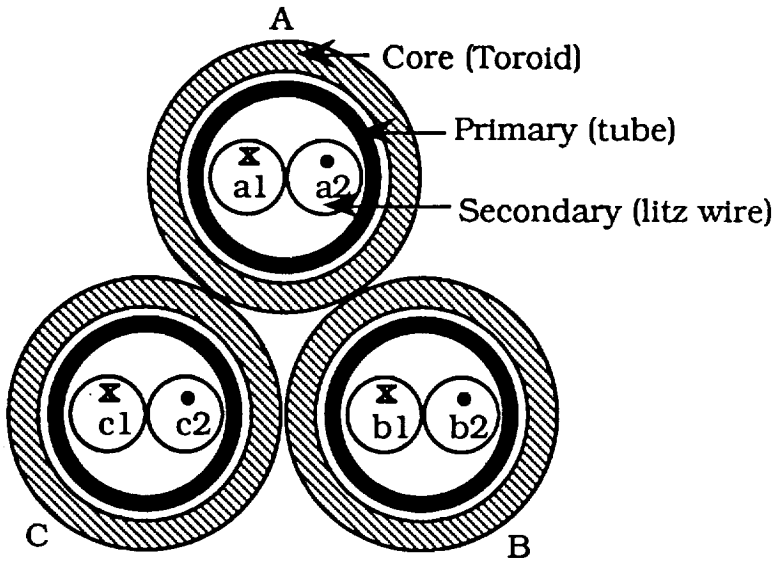


Fig. 7.6.4 Cross-section of a 3-phase coaxially wound Y-Y transformer, with "zig-zag" secondary.

weight and wide range of shapes. The influence of the leakage flux distribution, in the window region, on the copper losses has been demonstrated for various conventional winding arrangements. It is seen that in conventionally wound transformers, a considerable amount of leakage flux enters the core resulting in localized core saturation and hot-spots. This becomes a very critical issue especially for high-power high-frequency transformers. Coaxially wound transformers are seen to be a viable alternative, in that, the leakage flux is contained within the interwinding space, with very little or none of it permeating the core. Such transformers can also realize multiple benefits of a low distributed and controllable leakage inductance, robust construction, low electromechanical forces and low core and copper losses. Test results on two coaxially wound transformers, with different tube geometries, designed for 50 kW, 50 kHz, primary voltage of 200 V and secondary voltage of 1000 V (two windings) are presented. Finally, the concept of coaxial winding techniques for three phase transformers is also presented.

CHAPTER 8

EXPERIMENTAL VERIFICATION

8.1 Introduction

A prototype converter was designed and fabricated for the given specifications, based on the selected single phase dual active bridge dc/dc converter(Topology B). The converter was packaged for proper electrical and thermal management, with the intention of reducing system parasitics (stray inductances and capacitances), enhancing power density (in terms of both weight and volume) and maximizing cooling surface. Various experimental results under pulsed and continuous power flow at near rated conditions are presented. Finally, limitations of the converter driven primarily from inherent device characteristics are indicated.

8.2 Converter Specifications

Output Power, P_o = 50 kW

Input Voltage, V_i = 200 Vdc

Output Voltage, V_o = 2000 Vdc

Power Density = 0.2 - 0.3 kg/kW

Switching Frequency, f = 50 kHz

The choice of the switching frequency is primarily based upon the switching speeds and losses of the state-of-the-art switching devices and transformer losses at the power levels of interest.

8.3 Converter Design

As stated earlier, the high output voltage and high power density requirements mandate a series modular approach for the output stage, as devices rated in the kilovolt range are limited in terms of switching speed. For the specified output voltage, a cascaded connection of two active half-bridges is implemented, as shown in Fig. 8.3.1. The corresponding upper and lower devices of the two secondary side half-bridges are gated simultaneously to achieve identical phase-shifts from the input bridge. Note, other modes of control involving independent control of the two half-bridges with different phase-shifts can be implemented, but is beyond the scope of this thesis. The design and selection of the various components, outlined below, are based on the desirable operating point of $d = 1$, $\phi \approx 30°$ presented earlier in Table 5.2.1.

Transformer :

The rectangular coaxial transformer (design and constructional details presented in the Chapter 7) was implemented in the prototype converter primarily for its lower losses and compactness.

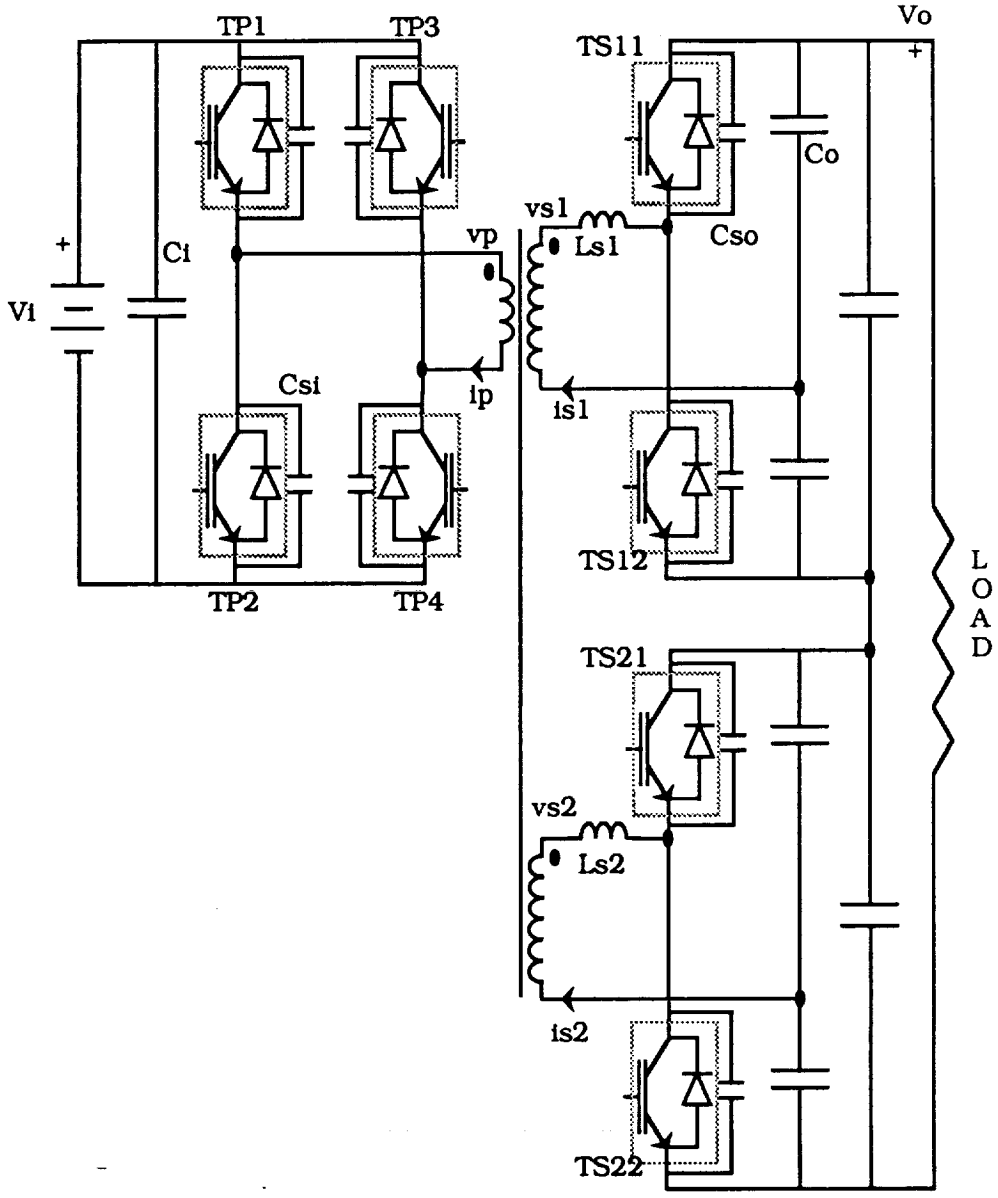


Fig. 8.3.1 Schematic of the single-phase dual active bridge dc/dc converter with series connected half-bridges on the output for high voltage.

Two modifications were necessary. Firstly, to account for the voltage doubling effect from the half-bridge arrangement on the output side and allow a 20% margin of safety on the voltage ratings of the switching devices and filter capacitors, the number of turns on each secondary winding was reduced to 6 (number of primary turns = 3). The output dc voltage requirement under rated operating conditions was thus brought down to 1600 Vdc. The higher secondary currents also required a lower gauge, AWG #6 Litz wire, to maintain the same operating current density of 5.83×10^6 A/m^2. The short-circuit copper losses were measured as 250W.

Secondly, the leakage inductance (primary-referred) required at the design point (d=1, ϕ=30°) and rated power is calculated from the output power relation,

$$P_o = \left[\frac{V_i^2}{2\pi f L}\right] d\phi \left[1 - \frac{|\phi|}{\pi}\right]$$

where, $d = \dfrac{V_o}{2NV_i}$

as L = 1.1 μH. However, the leakage inductance of the transformer was measured as 150 nH. The additional inductance required was incorporated in each of the two secondary windings to reduce interactions between the windings. L_{s1}, L_{s2}, shown in Fig. 8.3.1 are the two separate air-cored inductors, 4.3 μH each (1.07μH primary-referred), added in series with the windings.

Switching Device :

An ideal candidate for the application is the MOS-Controlled Thyristor(MCT), popularized for its high switching speed and low on-state voltage. However, given the fact that the technology is still in its "embryonic" stage, the availability and performance of the devices at these power levels is still not clear.

The next best alternative, which is the device of choice at this time, is the Insulated Gate Bipolar Transistor(IGBT) which combines the best of the MOS and Bipolar technologies. The desirable features of the device include :

(1) Relatively high switching speeds compared to the Bipolar Junction Transistor(BJT) at the power levels of interest

(2) High current densities, requiring less die area compared to the BJT

(3) MOS-gating, thus requiring compact and efficient gate drivers.

Two major drawbacks in the current technology are the higher continuous on-state voltage drop (giving higher conduction losses) and the appreciably large turn-on voltage, commonly referred to as "dynamic saturation" (resulting in turn-on switching losses).

For the given specifications and selected design point the peak turn-off current for the input bridge devices is 300 A and that for the output bridge is 75 A. To meet these ratings, with an additional safety factor of 20%, the input devices (TP1-TP4) are selected as

600V, 400A single device modules, and the output devices (TS11-TS22) as 1200V, 100A half-bridge modules.

DC Bus High Frequency(HF) Filter Capacitors :

For the prototype converter the state-of-the-art Multi-Layer Ceramic (MLC) capacitors were used, which offer high energy density, very high r.m.s. current handling capability at high frequency, very low Effective Series Resistance (ESR) and Effective Series Inductance (ESL) at the frequencies of interest. Conventionally used commutation-grade capacitors have comparable r.m.s. current carrying capacity, but are bulky and less amenable to high power density packaging.

Input Bridge HF Filter Capacitor (Ci) : At the design point, the input filter r.m.s. current is 130 A. The manufacturer's (Olean Advanced Corporation, AVX Division) specify 50 Arms capability for a typical 8-10μF, 500V part at 25°C. Allowing for a 40°C temperature rise, with some overengineering, the total filtering is implemented with 6x10μF, 500V and 2x8μF, 500V MLC capacitors.

Output Bridge HF Filter Capacitor (Co) : For a total filtering requirement of 35 Arms, each half of each output half-bridge is implemented with 2x8μF, 500V MLC capacitors. Moreover, to decouple the effects of any stray inductances an additional 2x8μF,1500V MLCs is mounted across each half-bridge.

Snubber Capacitors :

Based on the peak turn-off current at the design point, and a typical device tail time, t_f = 0.8μs and K = 0.25 (see IGBT Turn-off model in Chapter 4), the required critical value of snubber capacitance is calculated from eqn. (4.2.2). Since the snubber capacitors carry a substantial amount of r.m.s current, good quality capacitors with very low ESRs and ESLs are essential. Silvered-mica type have these desirable characteristics.

Input device snubber capacitor (Csi) : For a peak turn-off current of 300A, clamp(bus) voltage of 200V, and the given device turn-off specifications, the snubber capacitance(with 25% oversnubbing) is estimated as 0.55μF / device. The required r.m.s. current is calculated as 15% of peak turn-off current, which is 50Arms. This is implemented with 11x50,000pF, 500V Silvered-Mica capacitors.

Output device snubber capacitor (Cso) : At the operating point, the output devices turn-off a current 4 times(2 x N) smaller than the input device. Also, the clamp voltage is 4 times larger. Hence, the snubber capacitance required (assuming identical device turn-off characteristics) is 16 times smaller, which amounts to 0.04μF / device, for an r.m.s. current rating of 11Arms. This is realized with 4x10000pF, 1000V Silvered-mica capacitors.

8.4 Converter Layout

Crucial to the performance of high power density converters is its layout. As one move towards higher switching frequencies, stray inductances and capacitances (commonly referred to as parasitics) start to influence the performance of the converter. For the converter of interest, the dominant stray inductances and capacitances and their influence on performance are identified :

(1) Transformer leakage inductance - Used to advantage

(2) Inductance in device conduction path - Harmful

(3) Inductance introduced from bus connections - Harmful

(4) Device output capacitance - Used to advantage for ZVS

Stray inductance internal to the device (or the anti-parallel diode) can only be minimized by proper packaging of the device during manufacture. A point worth mentioning is that many manufacturers tend to overlook internal package inductances even in high speed devices like the IGBT, which ultimately limit the inherent current switching capability of the semiconductor. The adverse impact of package inductance on the efficiency of the converter is illustrated by a simplified model in a later section.

Figure 8.4.1 shows the layout of the 50 kW, 50 kHz prototype converter, fabricated in the laboratory. The schematic of the converter is shown in Fig. 8.3.1. All device-to-device power

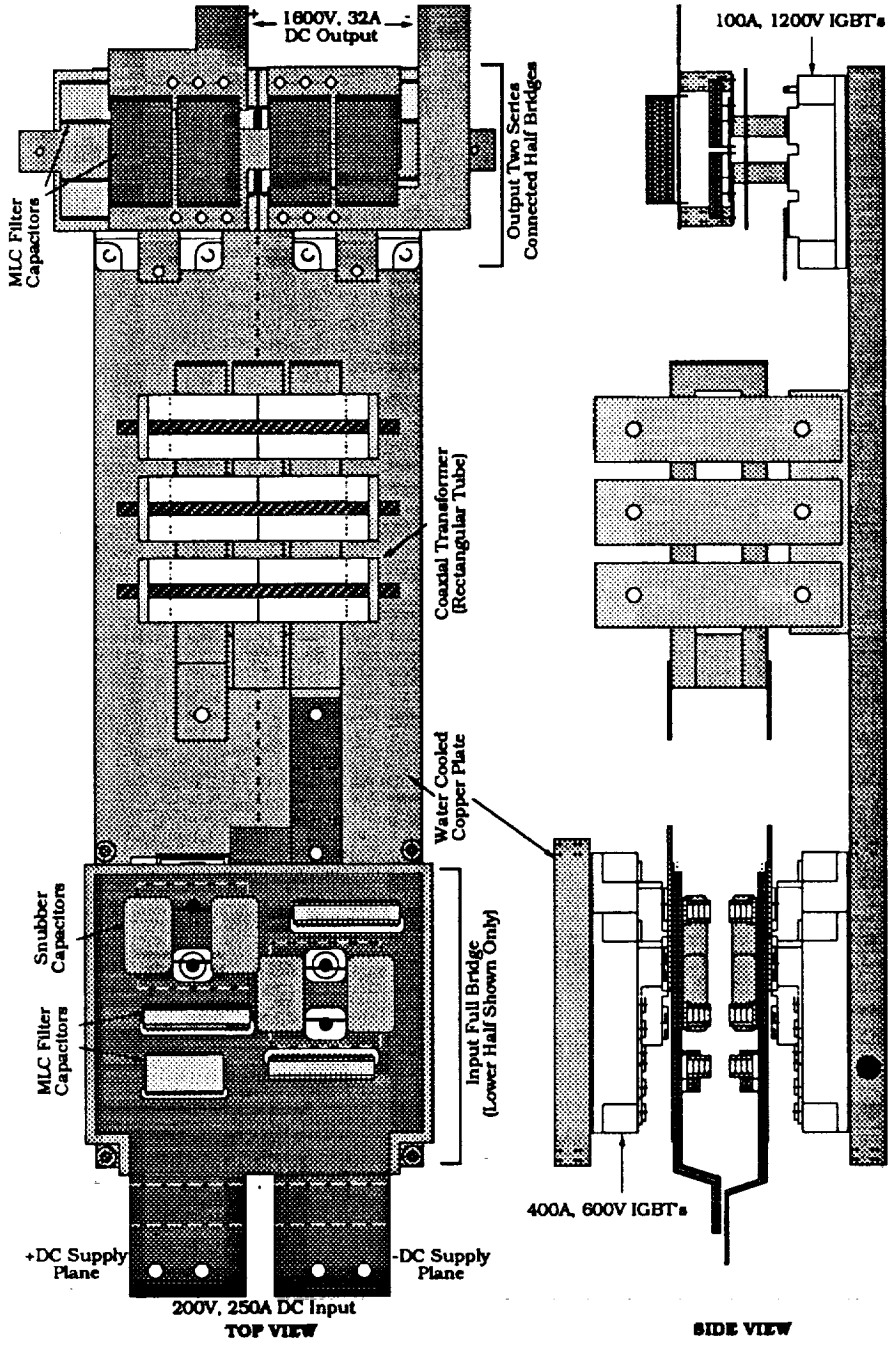


Fig. 8.4.1 Layout of the 50 kW, 50 kHz dual active bridge dc/dc converter.

connections and device-to-bus connections on both the bridges are made from multi-layer copper planes (32 mils thick). The planes are insulated from each other using kapton (5 mil). The planar approach allows a substantial reduction in stray inductances. Moreover, the high frequency MLC filter capacitors are distributed uniformly over the multi-layer planar busses to provide additional capacitive decoupling. The entire assembly of the planar busses with the distributed filter capacitors forms a tight, electrically "clean" structure. Also, the large surface area available for cooling makes thermal management easier and helps quickly spread the heat from the high current connection points.

To reduce the total footprint, all filter and snubber components on each bridge are arranged in a vertical stack moving on up from the device modules. On the input side, each inverter leg with its planar bus assembly is mounted on separate water-cooled copper plates. The lower water-cooled copper plate cools one leg of the input bridge, transformer cores and the two output half-bridge devices. The smaller water-cooled copper plate cools only the other leg of the input bridge and is supported symmetrically above the lower leg. The positive and negative dc supply planes from each inverter leg are brought out at one end. The hardware for the water-cooling system is not shown in the layout. Temperature sensors are mounted (also not shown in the layout) on the various components to monitor their temperature rise and identify their thermal stresses.

For overcurrent protection, a LEM current sensor mounted on the primary winding of the transformer, provides the shutdown signal.

Appendix E (Fig. E.2) shows the circuit schematic of the gate driver. Each driver card has its own isolated and regulated power supply. The logic level gating signal is fiber-optically isolated from the gate drive to ensure a high degree of immunity of the controller board from dV/dt noise generated at the gate-emitter terminals of the switching device. This is especially important at the high voltage side of the converter. The drive signal is bipolar, with +13V for on-drive and -5V for off-drive. It may be noted that higher on-drives, typically 15 to 18 V, would result in lower on-state voltages of the switching device, but the Teledyne driver chips (TSC4429) implemented have limited rail-to-rail voltage excursions.

Table 8.4.1 lists the components with their actual weights. The weight power density of 0.243 kg/kW meets the specified target of 0.2-0.3 kg/kW. However, the power density of the transformer alone is 0.08 kg/kW. It is thus seen that the overall power density is dominated by device package weight. Accounting for only the silicon weight and the device terminal connections (which has been estimated as 25% of the total package), the power density figure is projected as 0.2 kg/kW. The overall converter volumetric density is 80 W/cu.in. As a comparison, it is appropriate to mention here that the series resonant converter [2], using thyristors as devices, commutation-grade capacitors for the filters and Permalloy-80 core

Table 8.4.1

(Summary of Component Weights)

(P_O = 50 kW ; V_I = 200 Vdc ; V_O = 1600 Vdc ; f = 50 kHz)

Component	Description	Unit Wt. (gm)	Qty	Total Wt. (gm)
Input Full Bridge				
Switching Device (IGBT)	FUJI:1MBI400-600, 400A/600V	516	4	2064
H.F. Filter Cap. #1 (MLC)	SM017C106KHN480, 10μF/500V	35	6	210
H.F. Filter Cap. #2 (MLC)	SM027C805ZAN240, 8μF/500V	28	2	56
Snubber Cap. (Silver-mica)	CD42FD503J03, 50000pF/500V	34	44	1496
Gate Drivers	In-house, w/60Hz transformer	160	4	640
DC Bus Planes + Hardware	32mil Copper	160	4	690
Output Cascaded Bridges				
Switching Device (IGBT)	FUJI:2MBI100-120, 100A/1200V	386	2	772
H.F. Filter Cap. #1 (MLC)	SM027C805ZAN240, 8μF/500V	28	8	224
H.F. Filter Cap. #2 (MLC)	HV06SC805KAN650, 8μF/1500V	118	4	472
Snubber Cap. (Silver-mica)	CDV30FF103JO3,10000pF/1000V	15	20	300
Gate Drivers	In-house, w/60Hz transformer	160	4	640
DC Bus Planes + Hardware	32mil Copper (assorted sizes)			460
High Frequency Link				
Transformer (Rect. Coax.)	Turns ratio : 3,6,6		1	3660
Input Bridge Connections	32mil Copper	84	2	168
Series Inductor(Sec. Side)	Air-Core	150	2	300
Total Weight				**12152**
Power Density at 50 kW	**0. 243 kg/kW (80 W / cu. in.)**			

transformer has an overall power density of 0.9 kg/kW, for the same power rating.

8.5 Description of Controller

As stated earlier, the primary objective of this study is to develop a suitable topology for a high-power, high-frequency dc/dc converter and to demonstrate through a working model its performance at the power levels of interest. With this in mind, an open loop phase-shift controller was breadboarded to operate the converter in various modes of operation including continuous and pulsed power flow both in the forward and reverse directions. For bi-directional power transfer, capacitive energy storage banks are installed at the input and output. Appendix E (Fig. E.1) shows the details of the controller. Relevant logic level waveforms showing the various modes of operation and the synthesis of the gating signals are shown in Fig. E.3 (Appendix E).

Since the converter operates at a fixed switching frequency with symmetrical square waves on both the input and output, the controller logic is very simple and elegant. A signal, P, generated from the zero-crossings of a triangular wave (V_Δ) (running at the operating frequency) determines the switching of the leading bridge. In the forward power transfer mode, when P is at logic level '1', device-pair TP1,TP4 on the input bridge are gated on, and

conversely, when P is low device-pair TP2,TP3 are gated on. Signals δ_{XX} ensure a fixed dead time (δ) of 1μs between the complementary gating of the devices on the same leg. The fixed dead time is implemented to prevent shoot-through and also allow the snubber resonant transitions to be completed. Of course, during lightly loaded conditions this time may not be sufficient for the rail-to-rail resonant transitions, and the devices may experience a snubber discharge. A more elegant approach would involve gating of the device after the switch voltage has reached near zero. The sensing of the switch voltage could be incorporated into the gate drive.

A variable dc signal $V_{\phi M}$ compared with V_{Δ} determines the phase-shift, ϕ, between the input and output bridges. For instance, for $V_{\phi M} = 0$, $\phi = 0°$, and for $V_{\phi M}$ = peak of V_{Δ}, $\phi = 90°$. The logic signal S thus generated controls the switching of the output half-bridges. During reverse power flow, the roles of P and S are interchanged. Note, for different loads the range of ϕ must be maintained to operate within the soft-switching region. The following sections present operating waveforms and efficiency figures for the various modes of operation, under different load conditions.

8.6 Experimental Results

8.6.1 Forward Power Transfer

To test the converter at rated power conditions two approaches are adopted, primarily driven from the lack of a high-

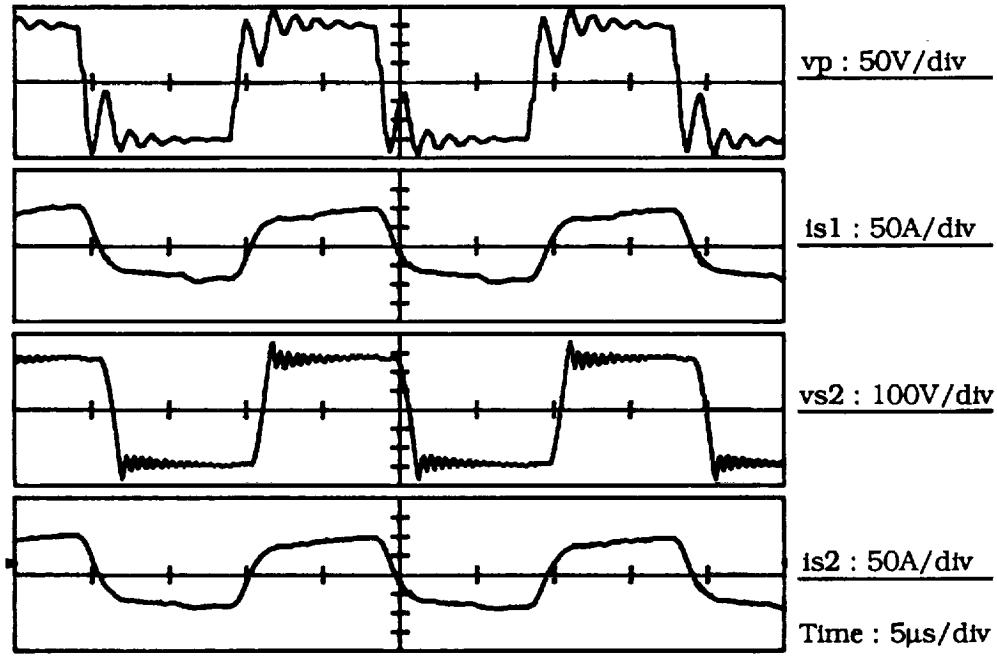
power, high-voltage load bank at our facility. In the first approach the converter is operated in a pulsed mode, where the average power delivered to the load is a fraction of the rated load, while the converter is carrying full power on a switching cycle basis. The low frequency pulse signal is also duty-cycle modulated to vary the effective load seen by the converter (Fig. E.3 and Table E.1, Appendix E illustrate the relevant controller signals for this mode of power transfer).

A 5 kW resistive load bank was assembled, and the pulse frequency was set to 100 Hz with a 10% duty-cycle, with the converter switching at 50 kHz. Theoretically, with the converter operating near the design point, the effective load seen should be 50 kW. Figs. 8.6.1a,b,c show the primary voltage(vp), one secondary voltage(vs1) and the two secondary currents(is1, is2) for a fixed load resistance of 307Ω, pulse duty-cycle of 10%, at three different phase-shifts. Fig. 8.6.1a depicts the case where the output bridges are operating as diode bridges, with the converter operating close to its lower soft-switching boundary (as seen on the Vo-Io plane). Relevant input and output dc quantities are mentioned in the figure. The total average power measured, on the secondary side of the transformer, over a switching cycle is 36.2kW, for an overall efficiency of 90.9%. The major contribution to the losses are seen to arise during turn-on of the input bridge devices, during which a large voltage drop is seen across the device. This is primarily governed by

two separate secondary effects - (i) dynamic saturation of the IGBT (device-physics dependent), and (ii) di/dt induced voltage in the internal package inductance in the device/diode conduction path. A later section briefly elaborates the two issues, and presents the projected improvement in efficiency in the absence of these secondary losses. The high frequency oscillations on the primary and secondary voltages can be attributed to the interactions between the package inductance and snubber capacitance.

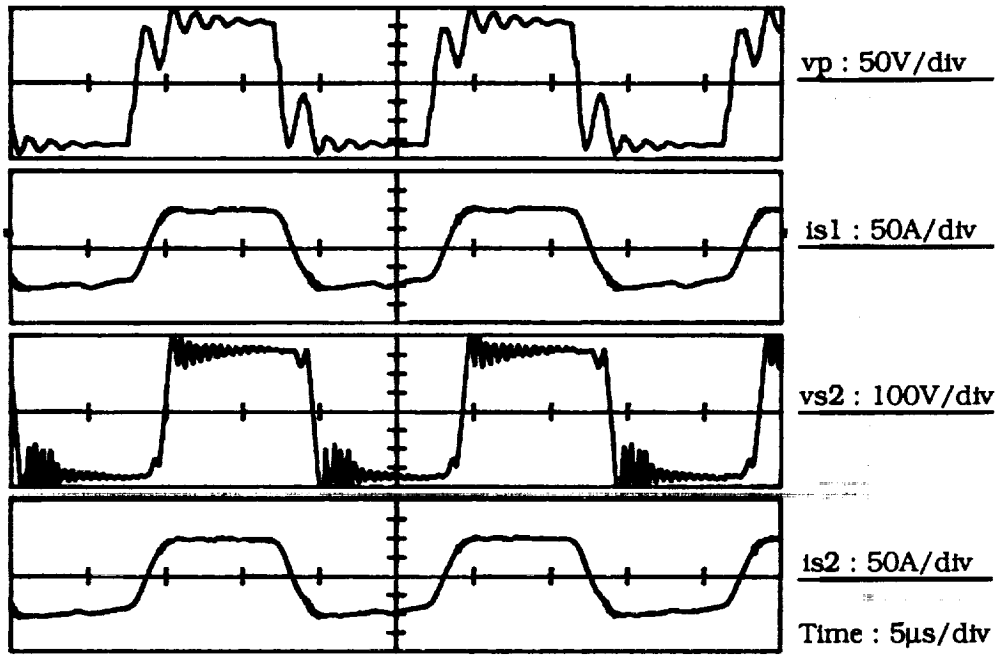
Fig. 8.6.1b shows waveforms obtained under the same load conditions, with the converter operating at a higher phase-shift of 41° and d = 1. The peak power seen by the converter is 48 kW, which is close to rated load. Also, the output bridge operates in the active mode as seen from the dynamic voltage drop on the secondary voltage waveform.

Fig. 8.6.1c shows operation in the boost mode at a phase-shift of 44°. Peak power measured in the converter is 49.4 kW. The efficiency drops as one moves from diode bridge to boost(active bridge) operation. This is expected since the conduction losses of the device are higher than that of the diode. Moreover, the additional turn-on and turn-off losses of the output device (during active mode of operation of the output bridge) also contribute significantly to the drop in efficiency. To repeat, the impact of the device package inductance on the efficiency and the resulting limitation on the



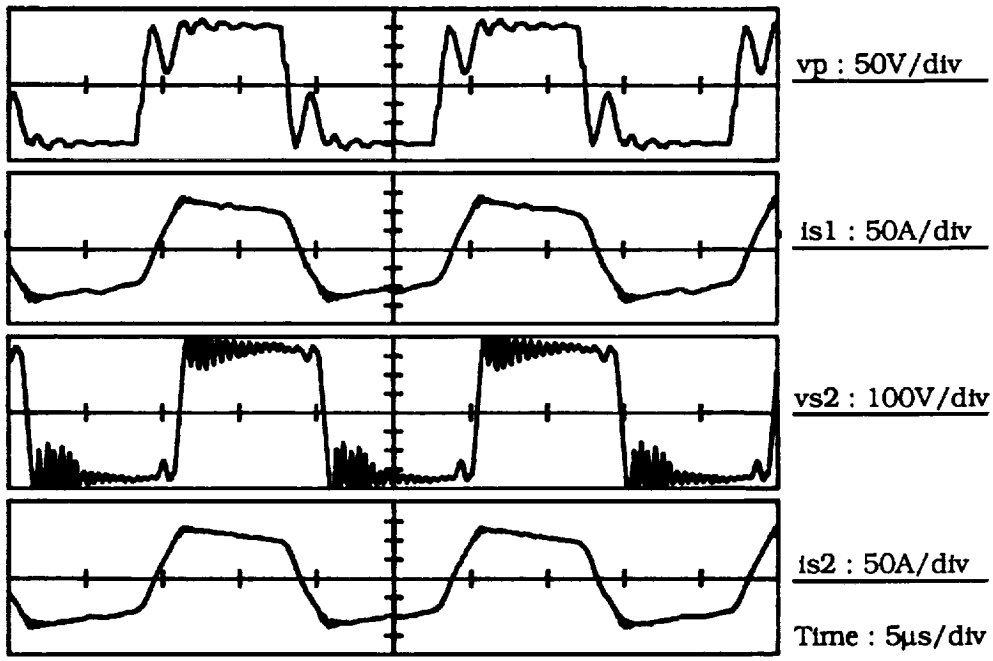
Frequency=50kHz, Load=307Ω(Resistor Bank).
Vi = 162Vdc, Ii = 26.8Adc, Pi = 4341.6W
Vo = 1096Vdc, Io=3.6Adc, Po=3946W
Overall efficiency = 90.9%
Average power per switching cycle, measured on the secondary side = 36.2kW.

Fig. 8.6.1a Forward power transfer under pulsed operation. Pulse frequency=100Hz, Duty cycle=10%. Output running as diode bridges.



Frequency=50kHz, Load=307Ω(Resistor Bank).
Vi = 170Vdc, Ii = 36.5Adc, Pi = 6205W
Vo = 1288Vdc, Io=4.2Adc, Po=5410W
Overall efficiency = 87.2%
Average power per switching cycle, measured on the secondary side = 48kW.

Fig. 8.6.1b Forward power transfer under pulsed operation. Pulse frequency = 100Hz, Duty cycle = 10%. Converter operating at d ≈ 1.



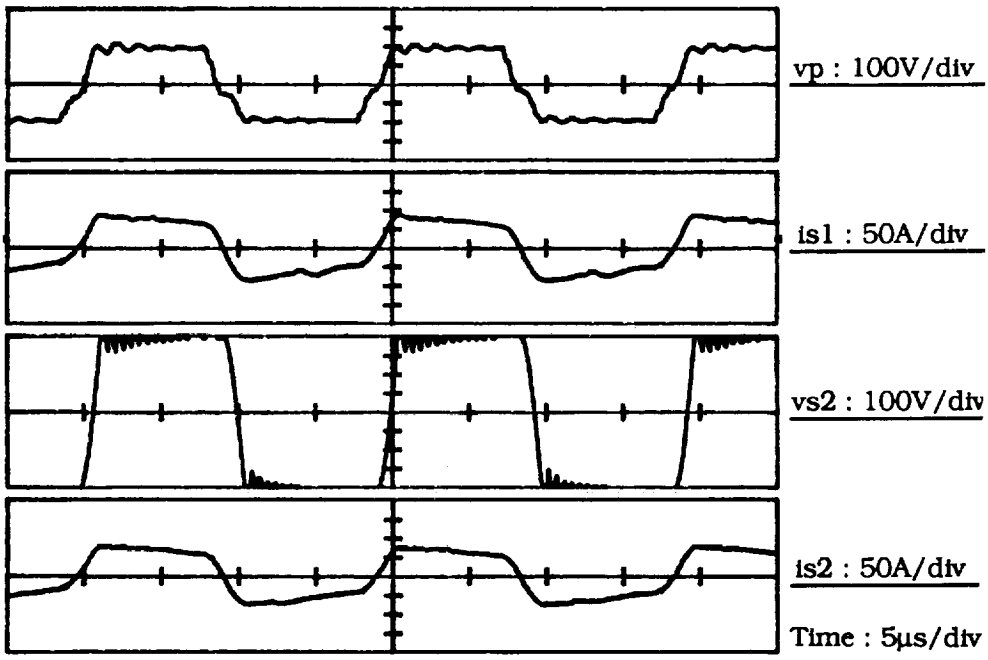
Frequency=50kHz, Load=307Ω(Resistor Bank).
Vi = 161Vdc, Ii = 40Adc, Pi = 6440W
Vo = 1301Vdc, Io=4.2Adc, Po=5464W
Overall efficiency = 84.8%
Average power per switching cycle, measured on the secondary side = 49.4kW.

Fig. 8.6.1c Forward power transfer under pulsed operation. Pulse frequency=100Hz, Duty cycle=10%. Converter operating in boost mode.

performance of the device must also be accounted for, as illustrated in a later section.

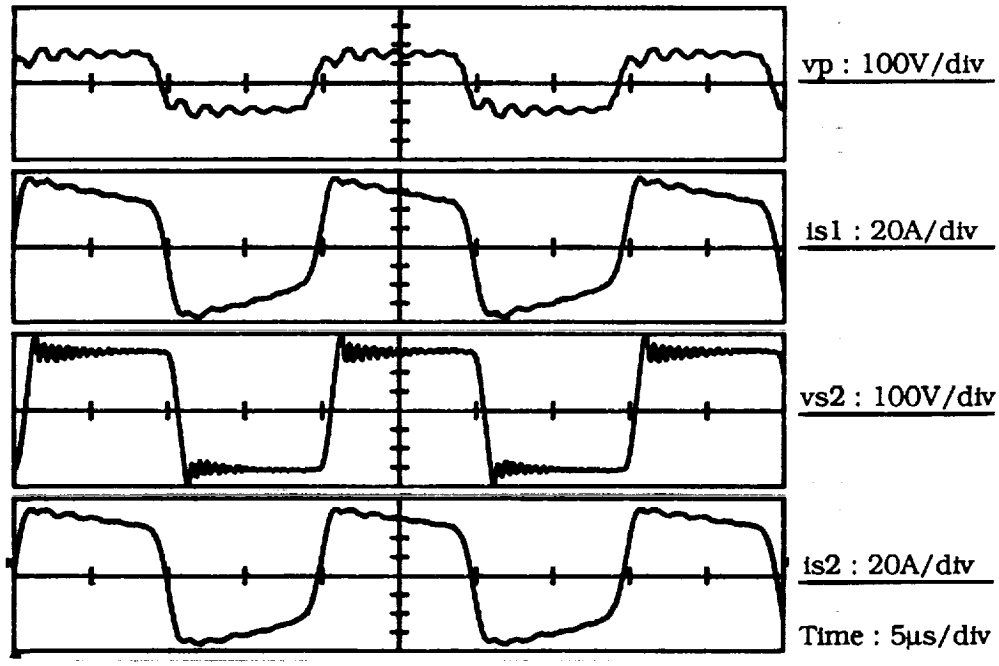
Fig. 8.6.2 shows the transformer waveforms at a higher load resistance of 574Ω, with the converter operating in the forward pulsed power transfer mode. The input and output dc voltages are near rated, at a peak power transfer of 46.2 kW.

Insofar as the peak power handling capability of the converter is concerned, the above test results validate the design of the converter from an electrical stress point of view. A 50 kW water-heating load is assembled to demonstrate the converter's thermal performance, specifically the transformer, the filter and snubber capacitors, since the cold plate is designed to water-cool the devices only. Eight water-heaters (rated for 4.5kW, 240V) are arranged in two parallel branches of 4 each in two 55-gallon barrels filled with water. The converter is operated for forward continuous power transfer. Fig. 8.6.3 shows the converter waveforms for an output power of 28.9 kW with the output bridge running as a diode bridge. Higher power outputs could not be achieved because of the limited capability of the input source. As seen from the temperature measurements (shown in the figure), after 5 minutes of operation, the transformer core and copper are thermally stressed the most. Proper forced-air or liquid-cooling is necessary for the transformer. Transformer design also needs to be optimized for lower copper



Frequency=50kHz, Load=574Ω(Resistor Bank).
Vi = 195Vdc, Ii = 25Adc, Pi = 4875W
Vo = 1600Vdc, Io=2.9Adc, Po=4640W
Overall efficiency = 95.2%
Average power per switching cycle, measured on the secondary side = 46.2kW.

Fig. 8.6.2 Forward power transfer under pulsed operation. Pulse frequency=100Hz, Duty cycle=10%. Output running as diode bridges.



Frequency=50kHz, Load=50.2Ω(Water Heater).
Vi = 152Vdc, Ii = 210.4Adc, Pi = 32kW
Vo = 1206Vdc, Io=24Adc, Po=28.9kW
Overall efficiency = 90.5%
Temperature rise : Primary winding : 162°F - 80°F = 82°F, Core : 140°F - 80°F = 60°F, Input MLC Filter Capacitors : 95°F - 80°F = 15°F, Input Snubber Silvered-Mica Capacitors : 98°F - 80°F = 18°F.

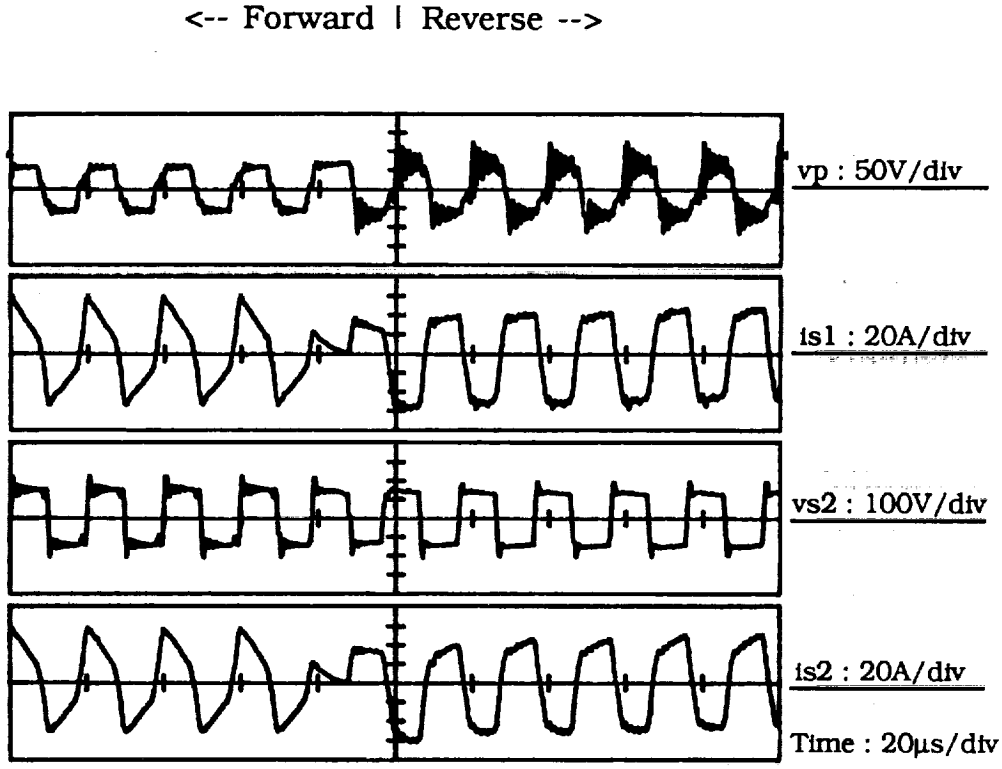
Fig. 8.6.3 Forward power transfer under continuous operation. Output running as diode bridges.

losses, with the use of high flux density materials like Permalloy-80. Snubber and filter capacitors with very low ESRs are desirable.

8.6.2 Bi-directional Power Transfer

The Vo-Io characteristic of the converter indicate that under light to no-load conditions the region of soft-switching is substantially reduced. This implies that in maintaining the output voltage under light loads, the converter may have to be hard switched. However, recognizing the bi-directional power flow capability of the converter, under these conditions, a "mode-hopping" strategy can be implemented, wherein the system is cycled sequentially between forward and reverse power transfer modes of operation to maintain the desired average output voltage. This allows the converter to still operate in the soft-switching region.

To demonstrate the bi-directional operation of the converter in an open-loop manner, the system is cycled 55% of the time in the forward mode and 45% in the reverse mode (see Appendix E for controller switch settings and relevant signals). Fig. 8.6.4 shows the converter waveforms for a low power condition. The phase-shift is 52°. Efficiency figure is not of concern because this mode of operation is only suitable under very light to no-load conditions. As seen the converter current adjusts from one mode to the other in half a switching cycle.



Frequency=50kHz, Load=905Ω(Resistive Bank).
Vi = 69Vdc, Ii = 45Adc, Pi = 3087W
Vo = 551Vdc, Io=0.8Adc, Po=441W

Fig. 8.6.4 Bi-directional power transfer. Pulse frequency=100Hz, Forward transfer : 55% of the time, Reverse transfer : 45% of the time.

8.7 Device Limitations

From the results presented in the previous sections, it is seen that the performance of the system is primarily limited by secondary effects associated with the switching device. These effects are identified as,

(i) Dynamic saturation of the IGBT, and

(ii) Stray inductances in device/anti-parallel diode conduction paths.

Fig. 8.7.1a shows a simplified steady state model of an IGBT [36,37], comprising an output bipolar PNP transistor driven by an n-channel MOSFET. When the device is gated on, the input MOSFET portion rapidly turns on. However, the output bipolar structure, being a conductivity-modulated device, requires a finite time in the order of the base carrier lifetime, before it goes into full conduction. This phenomenon, explained in certainly a very simplified manner, is referred to as dynamic saturation. The conductivity-modulated base resistance is shown in the model as a variable resistance.

The second factor contributing to the forward drop during turn-on and the increased losses is the stray inductance in the conduction paths. The situation worsens in the presence of high circuit di/dt's. The analysis below outlines the increased losses in the system due to these two effects, and projects the improvement in efficiency in the absence of these losses.

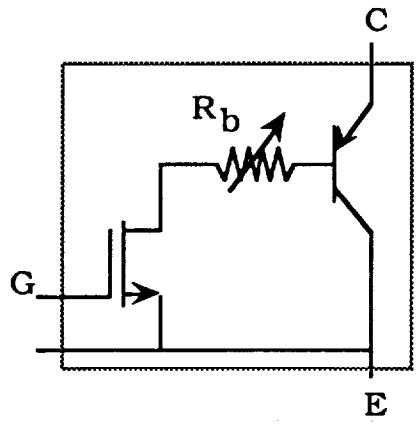


Fig. 8.7.1a Simplified equivalent circuit of the IGBT. R_b is the conductivity-modulated base resistance.

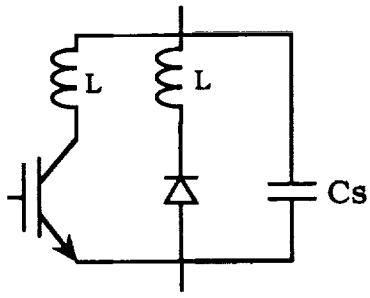


Fig. 8.7.1b Model of the switch showing the stray(package) inductances in the device and diode conduction paths. Cs is the snubber capacitance.

8.7.1 Device secondary-effect losses

The test result of Fig. 8.6.1b is considered as a case study. The stray inductance, L, in the device and diode conduction paths (shown in Fig. 8.7.1b) is measured as approximately 80nH for each of the input and output modules.

Loss due to device stray inductance at turn-off :

The initial rapid turn-off of the device causes the energy stored in the stray inductance of the device conduction path to be dissipated in the device. The total losses due to the stray inductance at turn-off for each bridge is given below.

Input bridge:

$$P_{SLi} = 4\ f\ (0.5\ L\ I_{mti}^2)$$

where, f is the switching frequency, L is the stray inductance in the device conduction path, I_{mti} is the peak current in the input device at turn-off. Referring to Fig. 8.6.1b, I_{mti} = 360A (4 times the peak secondary current, i_{s1}. The factor 4 accounts for the transformer turns ratio (1:2), and two secondary windings). L is measured as approximately 80nH. Hence,

$$P_{SL\_i} = 1036\ W$$

Similarly, the stray inductive losses for the secondary bridges are estimated as

$$P_{SL\_o} = 260\ W$$

Diode Reverse Recovery Losses :

During reverse recovery of the diode the energy stored in its the stray inductance is also dissipated. The peak reverse recovery current is calculated as,

$$I_{rrpk} = t_{rr} \frac{di}{dt}$$

where, t_{rr} is the reverse recovery current and di/dt is the rate of change of the diode current during turn-off. Hence, the stray inductive loss due to reverse recovery current is given as,

$$P_{rr} = f\left[0.5\, L\, I_{rrpk}^{2}\right]$$

For the manufacturer's specified t_{rr} of 150ns, the total reverse recovery losses for the input and output bridges are estimated as,

$P_{rr\_i} = 28$ W

and,

$P_{rr\_o} = 2$ W

As stated earlier, diode reverse recovery losses are a small fraction of the total device losses.

Device Turn-on Losses:

In zero-voltage switching applications, the device is expected to turn-on at near zero-voltage conditions, as the current flow reverses from the anti-parallel diode to the device. However, due to the slow turn-on process of the IGBT (referred to as dynamic

saturation), further aggravated by the device stray inductance, the load current finds a path through the snubber capacitance(see Fig. 8.7.1b). With the subsequent turn-on of the device, the energy stored in the snubber capacitance is rapidly discharged into the device, also resulting in the high frequency damped oscillations(due to interactions with the stray inductance) seen on the primary and secondary voltage waveforms of the results presented earlier. The device turn-on losses are computed from the energy stored in the snubber capacitance during turn-on, which is given as,

$$P_{dyn} \text{ / device} = 0.5\, C_s\, V_{CE}^2\, f$$

From Fig. 8.6.1b, V_{CE} for the input bridge device during turn-on is ≈50V(half the voltage-dip in vp during turn-on). Hence, the total turn-on losses for the input bridge (4 devices) is estimated as,

$$P_{dyn\_i} = 138 \text{ W}$$

Similarly, for the two output bridges,

$$P_{dyn\_o} = 48 \text{ W}.$$

The total losses due to the secondary effects is then,

$$P_L = P_{SL\_i} + P_{SL\_o} + P_{rr\_i} + P_{rr\_o} + P_{dyn\_i} + P_{dyn\_o}$$
$$= 1512 \text{ W}.$$

The peak power transferred over a switching cycle is measured as 47,990W at an overall efficiency of 87.2%. The projected efficiency in the absence of the above estimated secondary effect losses (P_L) is approximately 90%. Repeating the above analysis, for the boost mode of operation, Fig. 8.6.1c, the total secondary effect

losses are estimated as 2320 W. The projected efficiency is thus 88.3% an improvement of ≈4% from the measured efficiency of 84.8%.

The analysis thus reveals that a substantial degradation in the efficiency comes from the device secondary effects, most of which is contributed by the package stray inductance. It is thus important for device manufacturer's to pay a considerable attention to the package layout, especially for circuits intended to operate in the tens of kilohertz.

8.8 Summary

A 50kW, 50kHz dc/dc converter operating at an input voltage of 200Vdc and an output voltage of 1600Vdc is designed and fabricated. The converter is packaged for minimum layout electrical parasitics, good thermal management, high weight and volume power density. The choice of the switching device is the IGBT for its high switching speeds and low drive requirements. The overall power density of 0.243kg/kW meets the target specification of 0.2 - 0.3 kg/kW. The transformer, anticipated as the dominant component with respect to weight, has a power density of only 0.08kg/kW. The major weight penalty is seen to come from the device packaging.

Test results indicate that the converter is capable of handling peak power near rated conditions in a pulsed mode of power transfer at an overall efficiency in the range of 84-90%. Bi-directional mode

of power transfer at low power levels is also demonstrated. Limitations in the performance of the converter is shown to mainly arise from the device package inductance. A quantitative analysis for some test results indicates that a package inductance in the order of 80nH, degrades the overall efficiency by at least 3-4%.

CHAPTER 9

PROJECT SUMMARY AND CONCLUSIONS

9.1 Conclusions

The project was aimed at investigating the possibility of realizing high power density dc/dc converters suitable for multi-megawatt levels for aerospace applications, with the input power available at a few hundred volts, typical for fuel cell based systems. The output voltage was to be in the multi-kilovolt range, with the possibility of increasing that to hundred's of kilovolts. Ultimate power density goals of 0.1 kg/kW were critical and represented the most challenging of the many specifications. The magnitude of the task can be appreciated by noting that present day state of the converters, such as the series resonant converters, typically feature a power density of 0.9 kg/kW [2]. This project was aimed at advancing the state of the art and achieving a power density goal of 0.2-0.3 kg/kW.

Significant advances had to be made in a number of distinct and diverse areas before the desired specifications could be met. Some of the more obvious and important obstacles faced include the development of new power converter topologies and improved transformer structures suitable for high-frequency, high-power applications. During the course of the project, various other

important limitations were also identified and included the device internal packaging, converter packaging, transformer core materials and structures, heat transfer means, as well as parasitic inductances and capacitances within the system. This section compares the design of the converter with the performance obtained, and attempts to make projections on converters rated in the megawatt range as required in such applications. Some of the findings of this report are summarized in the following sections.

9.1.1 Converter Topology

Three new soft-switched dc/dc converter topologies have been proposed as being suitable for high frequency high-power applications. These are

(a)Single-Phase Single Active Bridge DC/DC Converter(Topology A)

(b)Single-Phase Dual Active Bridge DC/DC Converter(Topology B)

(c)Three-Phase Dual Active Bridge DC/DC Converter(Topology C)

The salient features of these topologies are :

1) Minimal structure, i.e., each consists of an input and output bridge, input and output filter capacitor, and a transformer, all components essential for a high power dc/dc conversion process.

2) Zero-voltage switching of devices allowing a reduction of device switching losses and hence, an increase in switching frequency.
3) Constant frequency operation, simplifying the design of the magnetic and filter elements.
4) Efficient use of system parasitics. The transformer leakage inductance is used for both energy transfer and zero-voltage switching along with the device output capacitance.
5) Operation of series/parallel connections of multiple modules for megawatt power levels
6) Low electromagnetic interference (EMI) as a result of limited dv/dt stresses.

In addition, Topologies B and C can realize,

7) Bi-directional power flow
8) Buck-boost operation
9) Reasonable component stresses at the rated operating point

The various steady state operating characteristics including, output voltage, power transfer, transformer utilization, filter capacitor kVA ratings and soft switching boundaries for converter operation are presented as a function of the control and load parameters. The major components of the converter losses, the device (switching and conduction) and transformer losses have been

characterized for the three topologies for various load and control conditions.

Topology A offers the possibility of realizing high output voltages without the use of series connected secondary stages, a result of the diode output rectifier stage. However, the input filter capacitor ratings and device stresses are much higher than those for Topologies B and C. On the other hand, Topologies B and C exhibit device VA stresses which are only 20% higher than that of an ideal hard switched pwm converter. Topologies B and C show substantially better transformer utilization compared to Topology A. As expected, the filter capacitor ratings for Topology C are the lowest.

Topology B is selected as a potential candidate for the following reasons :

1) Compared to Topology A, has wider range of control under soft-switching conditions.
2) Compared to Topology C, requires simpler transformer.
3) Although the filter-kVA requirements are higher than that for Topology C, the state-of-the-art high power density multi-layer ceramic capacitors, poses little or no additional weight penalty.
4) Compared to Topology A, incurs 33% lower device losses.
5) Compared to Topology C, requires fewer active devices, and hence fewer drive circuits.
6) The generic structure allows operation in Topology A mode, thus widening the region of soft-switching.

A fundamental component model for the dual active bridge topologies (B and C) is also presented which shows good correlation to the actual model. The model allows a better appreciation of soft switching constraints through phasor diagrams.

The influence of transformer magnetizing inductance and device snubber capacitance on the region of soft-switching are studied. It is shown that lower magnetizing inductance allows the devices to switch under zero-voltage conditions even at light to no load, at the expense of additional VA/watt. For increasing values of the device snubber capacitance, although the device switching losses decrease, the soft-switching region on the Vo - Io plane is reduced. However, it seems to be possible to select snubber capacitor and magnetizing inductance values such that the overall soft switching regime is not reduced. An alternative approach which seems feasible is the use of a mode-hopping strategy which cycles the converter alternately between forward and reverse power flow to maintain operation at an intermediate operating point.

9.1.2 Transformer Structure

It was realized right from the onset that transformer design would be one of the most critical factors affecting the realizable power density. Although a significant experience base exists in the area of low power high-frequency dc/dc converter transformer design, extension of those concepts to the multi-megawatt range

seems fraught with problems. For instance, core penetration of the leakage flux causes significant localized heating and results in oversizing of conventional geometry high frequency transformers. Flux penetration of copper foil windings causes significant additional copper loss. The leakage inductance, a crucial component in high frequency designs, is a parasitic in most transformers and cannot be accurately specified. Further for operation at high power and high frequency, the leakage inductance needs to be significantly lower than is possible with more conventional transformer geometries. Lastly, higher power densities require transformer designs which can easily accommodate forced heat removal strategies. Conventionally wound transformers with a cubical aspect ratio do not lend themselves to efficient heat transfer.

The co-axial transformer structure was seen to present a very attractive alternative at the relevant frequencies and power levels. Such transformers can realize multiple benefits of a low, distributed and controllable leakage inductance, robust construction, as well as low core and copper losses. Two such transformers, one with rectangular copper tubes and the other with circular tubes, have been assembled for rated power levels of 50 kW at 50 kHz. Efficiencies in the vicinity of 99%, and leakage inductance in the order of 150-250 nH have been measured. The power density obtained for the transformers was around 0.08 kg/kW, a significant improvement over conventional designs [38]. The transformer

designs fabricated and tested were not optimized in any way for electrical or thermal characteristics. As these were first examples of a newly evolving technology, the designs were based on simple extensions of manufacturers data. For instance, the flux levels were chosen from manufacturer data sheets. Copper conductor cross-sections were based on current densities used in conventional designs. Thermal effects were not a part of the transformer design process.

However, based on experience obtained with the two fabricated designs, and based on analytical work done since [39], it seems that significant improvements can be made in the transformer power density. The use of permalloy 80 or metglas cores could save on core weight, reduce transformer dimensions, and allow operation at higher temperatures than possible with ferrite cores. The transformer design using rectangular copper tubes was found to have exceptionally high copper loss, as a result of current crowding towards the center of the tube faces. The use of cylindrical tubular conductors for the outside winding is thus the preferred approach. Further, the almost cubical geometry of the rectangular tube transformer, although optimal for conventional transformers, is not preferred in coaxial designs [34,39]. On the contrary, a long and thin profile transformer is seen to be desirable on the basis of volume and weight power density, and minimum loss considerations.

The biggest problem with long and thin designs is the difficulty of porting copper losses out from the center of the long winding. The relative insensitivity of the leakage inductance (logarithmic dependence) to the inter-winding clearance suggests that this space could be intentionally enlarged and used for forced liquid cooling. This would allow a dramatic increase in the current density allowable in the transformer, possibly by as much as a factor of 3 - 4. This is normally a problem in conventional designs because the voltage droop across the leakage inductance at the elevated current levels is not acceptable. In the case of ultra-low leakage inductance coaxial designs, that is no longer an issue. It is projected that transformer power densities in the 0.03-0.05 kg/kW range are possible with further optimization in transformer design.

9.1.3 System Performance

A prototype system based on the selected Topology B, with series connected half-bridges on the output side, has been built for the rated specifications of 50kW, input and output dc voltages of 200V and 1600V respectively, and a switching frequency of 50kHz. The switching device used was the IGBT, as appropriately rated MCT's were not available. Device packages used were those available from commercial vendors, and were not optimized for high frequency operation. It has been mentioned that internal inductances in the order of 80 nH were a major limitation. Further, the devices

used were first generation IGBT's with forward voltage drops of 2.8 - 3 volts at rated current and significant dynamic saturation. Use of newer IGBT devices (with Vf = 2.2 volts) would result in much higher efficiencies.

A very important question which has been addressed concerns the use of active devices in a high voltage output environment. As fast active devices are not available at voltage ratings, it seems as if diode outputs would be preferrable. However, the high power density specification dictates the use of high frequency switching, which in turn requires fast diodes, typically not available with ratings of more than 1200 - 1600 volts. Consequently, even with diodes in the output bridge, one would need to series connect bridges in a 'voltage multiplier' arrangement to realize voltages in the tens of kilovolts. This is similar to the cascaded arrangement proposed and realized with the dual active bridge converter. It has been shown that multiple secondary bridges can be run off the same primary converter to realize higher voltages. This 'module', consisting of one primary converter, transformer and several cascaded secondary bridges, can then in turn be cascaded to realize even higher power levels. This approach is considered necessary because multi-megawatt power levels will only be realizable at the frequency levels of interest using modular converters rated at a few hundred kilowatts each.

The performance of the converter system was limited by several factors. The problem of increased loss in the devices due to internal inductances, dynamic saturation and high forward drop have already been addressed. Transformer losses, particularly for the rectangular tube version, were higher than anticipated as a result of proximity effects. One major limitation concerned the non-availability of adequately rated supply and load facilities in the laboratory. This prevented converter testing under rated conditions on a continuous basis. From the data obtained, it was observed that the converter comfortably delivered rated power of 50 kW, and up to 69 kW, while operating in a pulsed mode with a repetition rate of 100 hertz and a load duty factor of 10%. This indicates that the converter is electrically capable of delivering rated load.

Steady state tests for thermal performance gave rather mixed results. The devices were seen to operate without significant temperature rise and are considered adequate for the application. The maximum heat was seen to be generated in the transformer windings, for reasons listed above. Additional 'hot points' in the system were connection points, the ground and supply planes and snubber capacitor connection points to the ground planes. It seems that at the current levels present in the system, it is important to improve the means of making connections. The transformer was operated with 28 kW continuous output with a maximum temperature rise of 50°C. Given that there was no cooling for the

transformer, and that it was a first attempt design, it seems that obtaining the rated power level on a continuous basis should be entirely feasible. Loss reductions in the devices, snubber capacitors and transformer can only help to further improve the performance of the converter. It is projected that with low forward drop devices such as MCT's, and an optimized coaxial winding transformer, converter efficiencies of 95% should be obtainable.

9.1.4 Projections to Multi-Megawatt Levels

The original objective of this project was the realization of systems which could operate at high output voltages (10 - 100 kV) and high powers (1- 10 MW). The simultaneous goal of high power density has dictated the adoption of a modular approach. A very important question which has been repeatedly raised, and not answered here, is that of the optimum module rating in terms of power level and frequency. Although it was hoped that this issue could be addressed in the course of this project, the optimization seems to be rather complex and application dependent and should be the focus of a subsequent study.

On the basis of experience with the dual active bridge converter, one can make projections on the structure and power density of a full scale system. Fig. 9.1.1 shows the conceptual diagram for a base system consisting of a 1 MW converter with a 500 volt dc input and a 10 KV dc output. Each module would consist of a primary

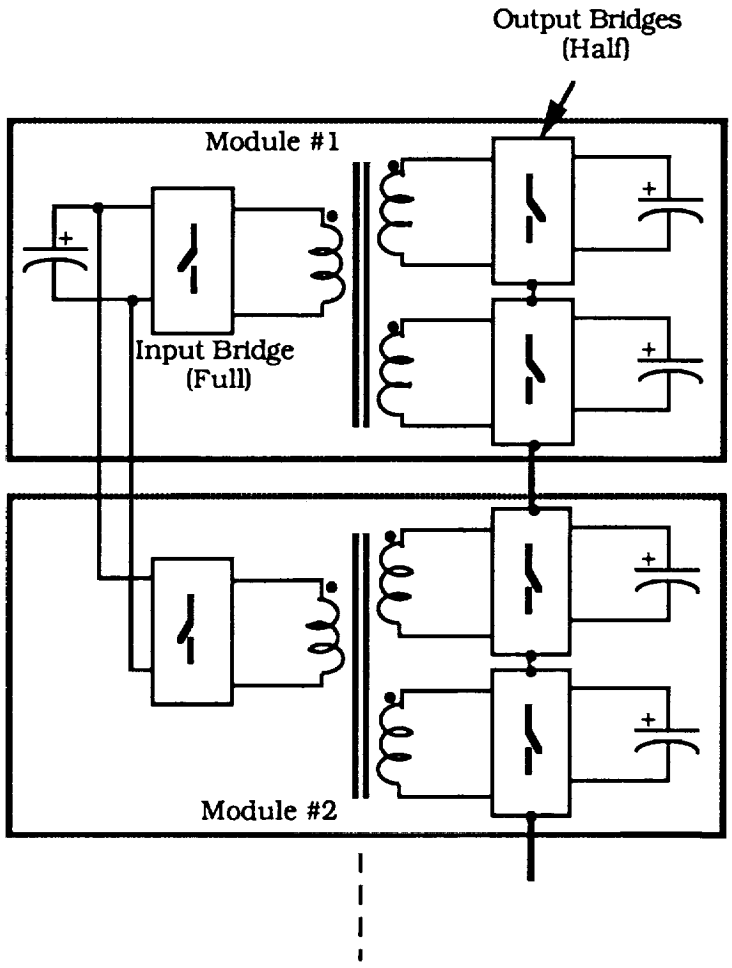


Fig. 9.1.1 Schematic of a 1 MW, 500 Vdc input, 10 kVdc output converter based on the dual active bridge topology. For this power level 6 Modules each rated for approximately 165 kW are required.

converter rated at approximately 165 kW. Thus there need to be six modules which operate in parallel off a common dc bus. As available fast active devices are presently restricted to 1200 volts, each secondary stage cannot be more than approximately 800 volts. Consequently, a total of at least 12 half bridge units are required in a series connection on the secondary side. These secondary converters are then distributed between the total number of modules used.

The devices are assumed to be MCT's with a Vf = 1.4 volts, and with low internal inductance, as well as low dynamic saturation voltage with zero voltage switching turn-on. Switching speeds for the MCT's are taken to be 1 μs for turn-off, which seems to be typical for presently available IGBT's. The transformer is assumed to operate at three times the present current density, given the availability of forced liquid cooling. This implies that the power density is reduced roughly by a factor of 2-3, while copper losses increase by a factor of 9. The frequency of switching is still assumed to be 50 kHz. With these assumptions, the losses are calculated to be 5800 watts for each module, giving a projected overall efficiency of 96%.

Weight calculations for the converter include devices, gate drives, filter capacitors, transformer, ground and supply planes as well as most of the mounting hardware. Device packages are assumed to be better than the 'brick' structure presently available. The use of direct bonded power device structures has recently been proposed, and seems to offer an attractive approach to reducing the weight of a

dominant component. These devices are assumed to weigh 125 gms each. The transformer weight for each module, given the forced cooling and improved core material is seen to be 3.8 kg for a 165 kW unit. The multi-layer ceramic input and output capacitors, and the snubber capacitors have been scaled from the present design. This suggests that an overall power density of 0.075 - 0.08 kg/kW can be achieved for the dual active bridge converter topology. Under similar operating constraints, the ultimate power density that can be achievable with the series resonant converter [2] is projected to be 0.147 kg/kW. Assumptions include similar component technologies including multi-layer ceramics, device weights and coaxially wound transformers. This suggests that the dual active bridge converter is potentially a viable converter topology for use at very high power levels if high power density is a primary design objective.

9.2 Future Work

This project has opened a wide range of possibilities in terms of continuing research efforts. The flexibility and scope of the proposed high-frequency, high-power dc/dc converters, especially the dual active bridge topologies, is such that considerable opportunities exist for further work in this area. Some of the more promising areas are identified below.

Independent Secondary Side Control : In the cascaded series-connected output bridges, independent current control for each secondary winding should be implemented to minimize interactions between the bridges, minimize any adverse effects due to mismatches between the leakage inductances and/or device parameters.

Optimal Switching Frequency : The choice of the switching frequency should be primarily based upon the constraints of high power density and high efficiency, which involves,

(1) Characterization of device-types for low switching and conduction losses

(2) Characterization of high-frequency core materials for operation at high flux densities and low losses

(3) Characterization of copper losses for various winding arrangements

(4) Assessment of possible sources of frequency-dependent parasitic ESR losses(filter and snubber capacitors, and layout)

(5) Assessment of possible lossy interactions of device stray inductances

(6) Assessment of regulator bandwidths for good transient response.

Coaxial Transformer Design with Forced Liquid Cooling : The possibility of operating coaxial winding transformers with large interwinding spaces raises the exciting prospect of providing forced

liquid cooling. Questions that need to be answered include factors which impact efficient heat removal, maximum coolant flow rates possible, means of cooling the core, and the possibility of higher temperature operation. Further, the optimal geometry of such a transformer also needs to be investigated.

Extension to Megawatt Power Levels : A typical approach for realizing power levels in the megawatt range is to parallel multiple identically rated low-power modules. The feature of current-controlled outputs in the proposed converter topologies, makes them very suitable for paralleling. Two areas of study are involved. Firstly, investigation of an optimum power module (for paralleling) based on constraints of device capabilities (speed, voltage and current), transformer size, losses and construction, filter size and losses, and thermal management. Secondly, issues related to independent control of the modules for minimum interactions and balanced load-sharing must be addressed.

Experimental Investigation of Topology C : A prototype 3-phase dual active bridge converter should be fabricated to verify some of the performance characteristics theoretically predicted in this work. A major issue could be design of a high power density, symmetrical 3-phase transformer based on either conventional winding arrangements (presented in Appendix A) or coaxial winding arrangements (presented in Chapter 7).

Investigation of Device Packaging for Improved Power Density : As seen from the experimental investigation, the performance in terms of both power density and efficiency is limited by the device package. The techniques of Direct Bond Copper and Stripline (as used in microwave devices) packaging could be utilized for low stray inductance and good heat removal.

Control Under Lightly-loaded Conditions : It has been shown for the dual active bridge topologies that under light to no-load conditions the region of lossless control is strongly influenced by the transformer magnetizing inductance and the device snubber capacitance. Decreasing magnetizing inductance helps widen the soft-switching region, whereas increasing snubber capacitance (for reducing switching losses) reduces soft-switching region. If the converter is so designed that under low-load conditions the region of soft-switching is pinched-off then to maintain regulation of the output voltage the bi-directional property of the converter can be utilized to cycle between forward and reverse power transfer. However, issues regarding output voltage ripple, stability and efficiency need to be addressed under such a "mode-hopping" control strategy.

High-Frequency Power Distribution : Fig. 9.2.1 shows a schematic of a high-frequency power distribution system using the dual active bridge converters. Active converters are placed at various strategic locations of the transmission system. Lagging VARs

demanded by the line can be supplied from any of these active bridges. This allows transmission over long distances with little or no voltage loss along the line. Resistive drops can also be compensated for by operating in the boost mode. Issues of transmission line design and interactions with parasitic shunt impedances, must be addressed.

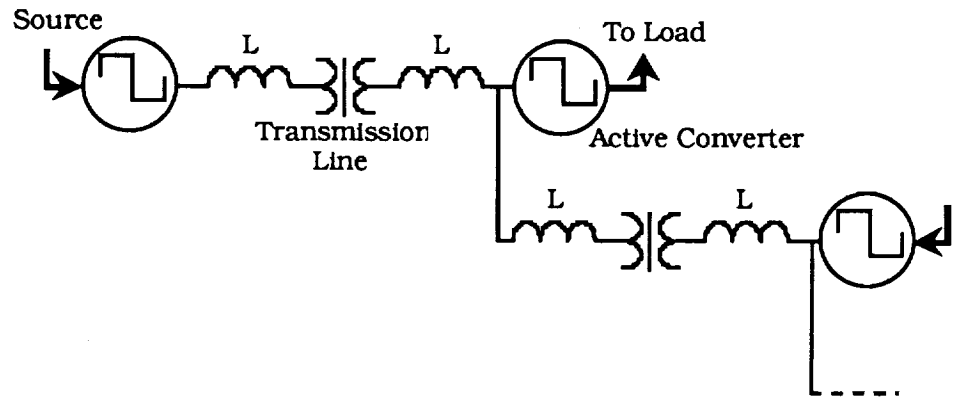


Fig. 9.2.1 High-frequency power distribution system.

CHAPTER 10

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APPENDIX A

Analysis of a 3-phase Symmetrical Y-Y transformer

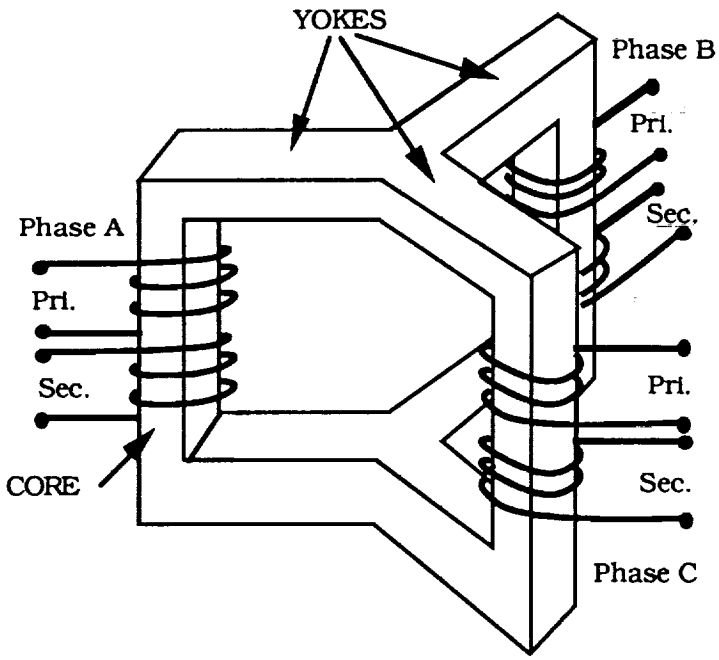

Fig. A.1 Schematic of a Symmetrical 3-phase Y-Y transformer.

Figure A.1 shows the schematic of a 3-phase symmetric transformer, for Topology C. The ac link transformer is Y-Y connected and is three phase symmetric with the leakage inductances used as energy transfer elements.

In the following analysis, it is assumed that the primary and secondary resistances of the transformer can be neglected and the

turns ratio is 1:1. Using the relationship $i_a + i_b + i_c = 0$ for Y connected transformers, the transformer equations can be derived as

$$V_{ap}(t) = L_{pl}\frac{di_{ap}}{dt} + \left[L_{pp}^{aa} + L_{pp}^{ab}\right]\frac{di_{ap}}{dt} + \left[L_{ps}^{aa} + L_{ps}^{ab}\right]\frac{di_{as}}{dt} \qquad \ldots(A.1)$$

and,

$$V_{as}(t) = L_{sl}\frac{di_{as}}{dt} + \left[L_{ss}^{aa} + L_{ss}^{ab}\right]\frac{di_{as}}{dt} + \left[L_{sp}^{aa} + L_{sp}^{ab}\right]\frac{di_{ap}}{dt} \qquad \ldots(A.2)$$

where V_{ap} and V_{as} are the primary and secondary voltages for the a-phase, L_{pl} and L_{sl} are the primary and secondary leakage inductances, L_{pp} and L_{ss} are self inductances and L_{ps}, L_{sp} are the mutual inductances between the appropriate phase windings given by the superscript notation used.

Using properties of a symmetric transformer and defining

$$L_m = L_{ss}^{aa} + L_{ss}^{ab} = L_{pp}^{aa} + L_{pp}^{ab} \qquad \ldots(A.3)$$

one can derive

$$\sigma(L_m + L_{sl})\frac{di_{as}}{dt} = V_{as}(t) - \frac{L_m}{L_m + L_{pl}}V_{ap}(t) \qquad \ldots(A.4)$$

$$\sigma(L_m + L_{pl})\frac{di_{ap}}{dt} = V_{ap}(t) - \frac{L_m}{L_m + L_{sl}}V_{as}(t) \qquad \ldots(A.5)$$

where, σ is a leakage factor given by

$$\sigma = \frac{(L_m + L_{sl}) (L_m + L_{pl}) - L_m^2}{(L_m + L_{pl}) (L_m + L_{sl})} \qquad \text{...(A.6)}$$

The value of σ is typically a small number approximately equal to the ratio of the leakage to the magnetizing inductances.

Equations (A.5) and (A.6) are the basic equations which govern the current in the circuit. Further assuming that $L_{sl} = L_{pl} \ll L_m$ (for 1:1 turns ratio), then these equations reduce to

$$L_\sigma \frac{di_{as}}{dt} = V_{as}(t) - V_{ap}(t) \qquad \text{...(A.7)}$$

$$L_\sigma \frac{di_{ap}}{dt} = V_{ap}(t) - V_{as}(t) \qquad \text{...(A.8)}$$

where,

$$L_\sigma = \sigma (L_m + L_{sl}) = \sigma (L_m + L_{pl}) = (L_{sl} + L_{pl}) \qquad \text{...(A.9)}$$

The simplified single equivalent circuit of the 3-phase transformer reduces to that shown in Figure 3.4.1b with $L = L_\sigma$. It can be seen that with the above assumptions, $i_{as} = i_{ap} = i(\theta)$.

APPENDIX B

Expressions for the device switching and conduction losses for the three proposed topologies

In the expressions below, the transformer turns ratio (secondary to primary) is assumed one. For a turns ratio of N, divide all output bridge conduction losses by N. The device switching losses are computed based on a snubber capacitance selected for critical snubbing at the maximum turn-off current seen by the device over a specified range of operation (see below for each topology). With the operating range specified the worst case snubber capacitance (for each bridge) and hence, the device switching losses are computed from eqns. (4.2.2) and (4.2.1) respectively. The following is the notation for the expressions below,

i_p (.) : Transformer primary current

V_I : Input dc voltage

f : Switching frequency, $\omega = 2\pi f$

t_f : Device fall time (see Figure 4.2.1)

K : Device fall parameter (see Figure 4.2.1)

L : Transformer primary-referred leakage inductance

d : DC voltage conversion ratio referred to primary side

β : Control parameter for Topology A

ϕ : Control parameter for Topologies B and C

θ_0 : Time instant at which i_p reverses direction from negative to positive

V_D : Diode Forward Drop

V_T : Device Forward Drop

$P_{sw(TX)}$: Switching Losses in Device TX of Input Bridge

$P_{sw(TX')}$: Switching Losses in Device TX' of Output Bridge

P_{sw_i} : Total Switching Losses in Input Bridge

P_{sw_o} : Total Switching Losses in Output Bridge

P_{DX} : Conduction Losses in Diode DX of Input Bridge

P_{TX} : Conduction Losses in Device TX of Input Bridge

$P_{DX'}$: Conduction Losses in Diode DX' of Output Bridge

$P_{TX'}$: Conduction Losses in Device TX' of Output Bridge

P_{co_i} : Total Conduction Losses in Input Bridge

P_{co_o} : Total Conduction Losses in Output Bridge

Topology A

Specified range of operation:

$0 \le d \le 1, \quad 0 \le \beta \le \pi$

Maximum turn-off current for input bridge occurs at $d = 0, \beta = \pi$

$$I_1 = i_p(0) = -\frac{V_i}{2\omega L}[(1 + d)(\beta - d\pi]$$

$$I_2 = i_p(\beta) = \frac{V_i}{2\omega L}[(1 - d)(\beta + d\pi]$$

Switching Losses :

Input Bridge :

$$P_{sw(T1)} = \frac{f^2 L t_f}{3}\left[\frac{4 - 3K}{2 - K}\right] |I_1|^2$$

$$P_{sw(T4)} = \frac{f^2 L t_f}{3}\left[\frac{4 - 3K}{2 - K}\right] |I_2|^2$$

$$P_{sw\_i} = 2\left[P_{sw(T1)} + P_{sw(T4)}\right]$$

Conduction Losses :

Input Bridge :

$$P_{D1} = \frac{V_D}{4\pi}\left[\phi\, |I_1|\right]$$

$$P_{T1} = \frac{V_T}{4\pi}\left[(\pi - \phi)\, |I_2| + (\pi - \beta)\, |I_1|\right]$$

$$P_{D3} = \frac{V_D}{4\pi}\left[(\pi - \beta + \phi)\, |I_1| + (\pi - \beta)\, |I_2|\right]$$

$$P_{T4} = \frac{V_T}{4\pi}\left[(\beta - \phi)\, |I_2|\right]$$

$$P_{co\_i} = 2\left[P_{D1} + P_{D3} + P_{T1} + P_{T4}\right]$$

Output Bridge:

$$P_{D1'} = \frac{V_D}{4\pi}\left[(\pi - \phi)\, |I_2| + (\pi - \beta + \phi)\, |I_1|\right]$$

$$P_{co\_o} = 4P_{D1'}$$

Topology B

Specified range of operation:

$$0 \le d \le 1.5, \quad 0 \le \phi \le \pi / 2$$

Maximum turn-off current for input bridge occurs at $d = 0$, $\phi = \pi / 2$

Maximum turn-off current for output bridge occurs at $d = 1.5$, $\phi = \pi/2$

$$I_1 = i_p(0) = -\frac{V_i}{\omega L}\left[d\phi + \frac{\pi}{2}(1 - d)\right]$$

$$I_2 = i_p(\phi) = \frac{V_i}{\omega L}\left[\phi - \frac{\pi}{2}(1 - d)\right]$$

$$\theta_0 = \frac{I_1 \phi}{I_1 - I_2}$$

Switching Losses :

Input Bridge :

$$P_{sw(T2)} = \frac{f^2 L t_f}{3}\left[\frac{4 - 3K}{2 - K}\right] |I_1|^2$$

$$P_{sw\_i} = 4\left[P_{sw(T2)}\right]$$

Output Bridge :

$$P_{sw(T2')} = \frac{f^2 L t_f}{3}\left[\frac{4 - 3K}{2 - K}\right] |I_2|^2$$

$$P_{sw\_o} = 4\left[P_{sw(T2')}\right]$$

Conduction Losses :

Input Bridge :

$$P_{D1} = \frac{V_D}{4\pi}\left[\theta_0 |I_1|\right]$$

$$P_{T1} = \frac{V_T}{4\pi}\left[(\pi - \theta_0)|I_2| + (\pi - \phi)|I_1|\right]$$

$$P_{co\_i} = 4\left[P_{D1} + P_{T1}\right]$$

Output Bridge :

$$P_{D1'} = \frac{V_D}{4\pi}\left[(\pi - \phi + \theta_0)|I_1| + (\pi - \phi)|I_2|\right]$$

$$P_{T1'} = \frac{V_T}{4\pi}\left[(\phi - \theta_0)|I_2|\right]$$

$$P_{co\_o} = 4\left[P_{D1'} + P_{T1'}\right]$$

Topology C

Specified range of operation :

$$0 \le d \le 1.5, \quad 0 \le \phi \le \pi / 2$$

Maximum turn-off current for input bridge occurs at d=0, $\phi=\pi/2$

Maximum turn-off current for output bridge occurs at d=1.5, $\phi=\pi/2$

Region I : $0 \le \phi \le \pi/3$

Primary phase 'a' current at the six switching instants of first half-cycle :

$$I_1 = i_p(0) = \frac{V_i}{9\omega L}\left[2\pi(d - 1) - 3d\phi\right]$$

$$I_2 = i_p(\phi) = \frac{V_i}{9\omega L}\left[2\pi(d - 1) + 3\phi\right]$$

$$I_4 = i_p(\phi + \pi/3) = \frac{V_i}{9\omega L}\left[\pi(d - 1) + 6\phi\right]$$

$$I_5 = i_p(2\pi/3) = \frac{V_i}{9\omega L}\left[\pi(1 - d) + 6d\phi\right]$$

$$I_6 = i_p(\phi + 2\pi/3) = \frac{V_i}{9\omega L}\left[\pi(1 - d) + 3\phi\right]$$

$$\theta_0 = \frac{I_1\,\phi}{I_1 - I_2}$$

Switching Losses :

Input Bridge :

$$P_{sw(T2)} = \frac{3\,f^2\,L\,t_f}{4}\left[\frac{4 - 3K}{2 - K}\right]|I_1|^2$$

$$P_{sw\_i} = 6\left[P_{sw(T2)}\right]$$

Output Bridge :

$$P_{sw(T2')} = \frac{3\,f^2\,L\,t_f}{4}\left[\frac{4 - 3K}{2 - K}\right]|I_2|^2$$

$$P_{sw\_o} = 6\left[P_{sw(T2')}\right]$$

Conduction Losses :

Input Bridge :

$$P_{D1} = \frac{V_D}{4\pi}\left[\theta_0 |I_1|\right]$$

$$P_{T1} = \frac{V_T}{4\pi}\left[\frac{\pi}{3}\left[\sum_{k=1}^{6} |I_k|\right] - \phi|I_1| - \theta_0|I_2|\right]$$

$$P_{co\_i} = 6\left[P_{D1} + P_{T1}\right]$$

Output Bridge :

$$P_{D1'} = \frac{V_D}{4\pi}\left[(-\phi+\theta_0)|I_1| - \phi|I_2| + \frac{\pi}{3}\left[\sum_{k=1}^{6} |I_k|\right]\right]$$

$$P_{T1'} = \frac{V_T}{4\pi}\left[(\phi - \theta_0)|I_2|\right]$$

$$P_{co\_o} = 6\left[P_{D1'} + P_{T1'}\right]$$

Region II : $\pi/3 \le \phi \le 2\pi/3$

Primary phase 'a' current at the six switching instants of first half-cycle :

$$I_1 = i_p(0) = \frac{V_i}{9\omega L}\left[3d(\pi - 2\phi) - 2\pi\right]$$

$$I_2 = i_p(\phi - \pi/3) = \frac{V_i}{9\omega L}\left[\pi d + 3(\phi - \pi)\right]$$

$$I_3 = i_p(\pi/3) = \frac{V_i}{9\omega L}\left[3d(\pi - \phi) - \pi\right]$$

$$I_4 = i_p(\phi) = \frac{V_i}{9\omega L}\left[2\pi\, d + 3(2\phi - \pi)\right]$$

$$I_5 = i_p(2\pi/3) = \frac{V_i}{9\omega L}\left[3d\phi + \pi\right]$$

$$I_6 = i_p(\phi + \pi/3) = \frac{V_i}{9\omega L}\left[\pi\, d + 3\phi\right]$$

Switching Losses :

Input Bridge :

$$P_{sw(T2)} = \frac{3\, f^2\, L\, t_f}{4}\left[\frac{4 - 3K}{2 - K}\right] |I_1|^2$$

$$P_{sw\_i} = 6\left[P_{sw(T2)}\right]$$

Output Bridge :

$$P_{sw(T2')} = \frac{3\, f^2\, L\, t_f}{4}\left[\frac{4 - 3K}{2 - K}\right] |I_4|^2$$

$$P_{sw\_o} = 6\left[P_{sw(T2')}\right]$$

Conduction Losses :

Case I : $\pi/3 \le \theta_0 \le \pi/2$

$$\theta_0 = \frac{\pi}{3} + \frac{I_3\left[\phi - \frac{\pi}{3}\right]}{I_3 - I_4}$$

Input Bridge :

$$P_{D1} = \frac{V_D}{4\pi}\left[(\phi - \frac{\pi}{3})\,|I_1| + (\frac{\pi}{3})\,|I_2| + (\frac{\pi}{3} - \phi + \theta_0)\,|I_3|\right]$$

$$P_{T1} = \frac{V_T}{4\pi}\left[(\frac{2\pi}{3} - \theta_0)\,|I_4| + (\frac{\pi}{3})\,|I_5| + (\frac{\pi}{3})\,|I_6| + (\frac{2\pi}{3} - \phi)\,|I_1|\right]$$

$$P_{co\_i} = 6\left[P_{D1} + P_{T1}\right]$$

Output Bridge :

$$P_{D1'} = \frac{V_D}{4\pi}\left[\frac{\pi}{3}\left[\sum_{k=1}^{6} |I_k|\right] + (\frac{\pi}{3} - \phi)\,|I_4| + (\theta_0 - \phi)\,|I_3|\right]$$

$$P_{T1'} = \frac{V_T}{4\pi}\left[(\phi - \theta_0)\,|I_4|\right]$$

$$P_{co\_o} = 6\left[P_{D1'} + P_{T1'}\right]$$

Case II : $(\phi - \pi/3) \le \theta_0 \le \pi/3$

$$\theta_0 = (\phi - \frac{\pi}{3}) + \frac{I_2\left[\frac{2\pi}{3} - \phi\right]}{I_2 - I_3}$$

Input Bridge :

$$P_{D1} = \frac{V_D}{4\pi}\left[(\phi - \frac{\pi}{3})\,|I_1| + \theta_0\,|I_2|\right]$$

$$P_{T1} = \frac{V_T}{4\pi}\left[(\phi - \theta_0)\,|I_3| + (\frac{\pi}{3})\,|I_4| + (\frac{\pi}{3})\,|I_5| + (\frac{\pi}{3})\,|I_6| + (\frac{2\pi}{3} - \phi)\,|I_1|\right]$$

$$P_{co\_i} = 6\left[P_{D1} + P_{T1}\right]$$

Output Bridge :

$$P_{D1'} = \frac{V_D}{4\pi}\left[\frac{\pi}{3}\left[|I_1| + |I_4| + |I_5| + |I_6|\right] + \theta_0 |I_2| + (\frac{\pi}{3} - \phi)\,|I_4|\right]$$

$$P_{T1'} = \frac{V_T}{4\pi}\left[(\phi - \theta_0)\,|I_3| + (\phi - \frac{\pi}{3})\,|I_4|\right]$$

$$P_{co\_o} = 6\left[P_{D1'} + P_{T1'}\right]$$

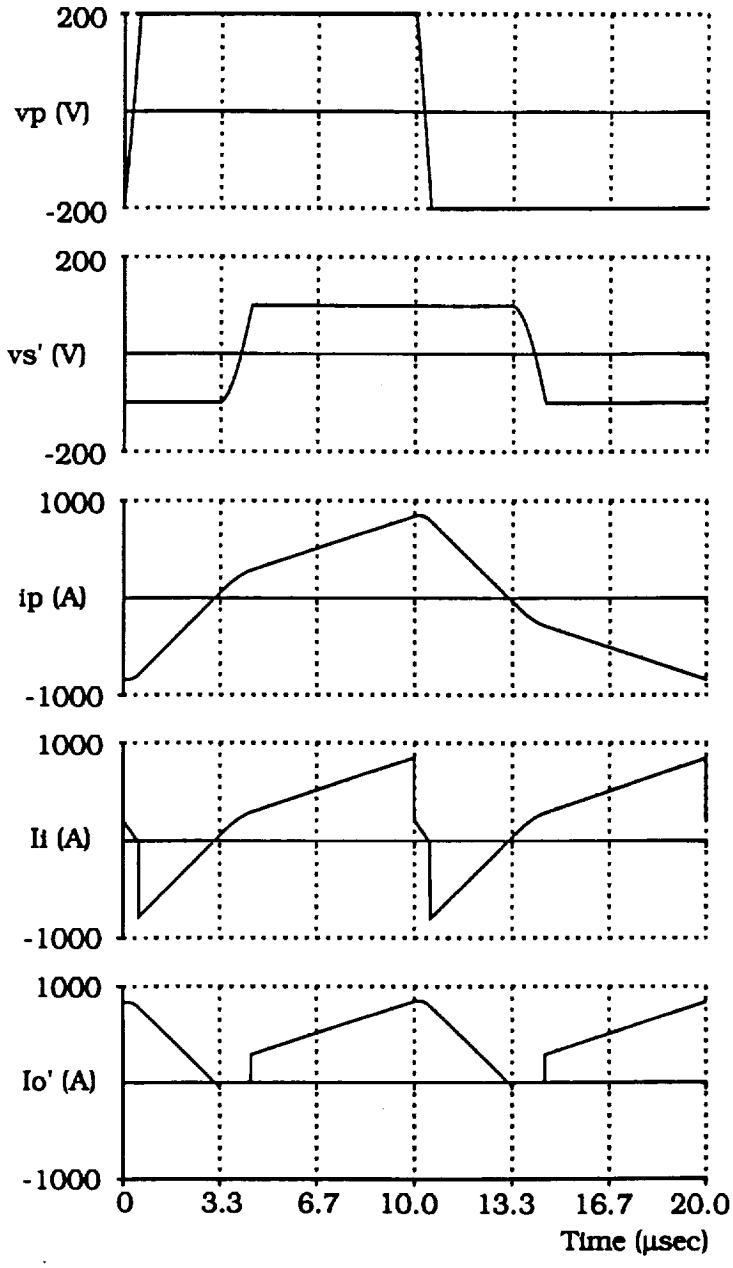

Fig. B.1a Simulated Topology B waveforms in the presence of finite snubber capacitors, with the device(IGBT) turn-off model. d=0.5(buck mode), ϕ=60°, V_I=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V, $C_i = C_o$ = 1μF (input and output snubber capacitors), L = 1μH.

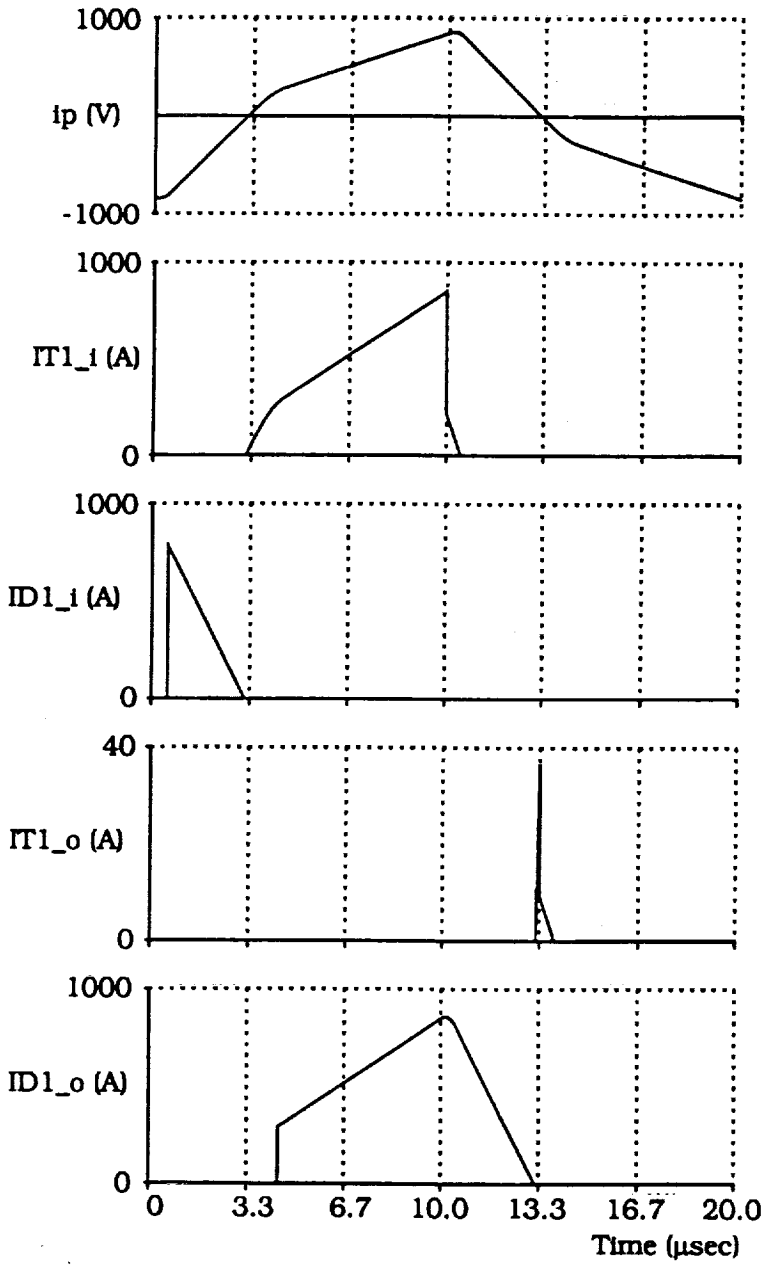

Fig. B.1b Simulated input and output device/diode current waveforms for Topology B, with the device(IGBT) turn-off model. d=0.5(buck mode), ϕ=60°, V_i=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V, C_i = C_o = 1μF (input and output snubber capacitors), L = 1μH.

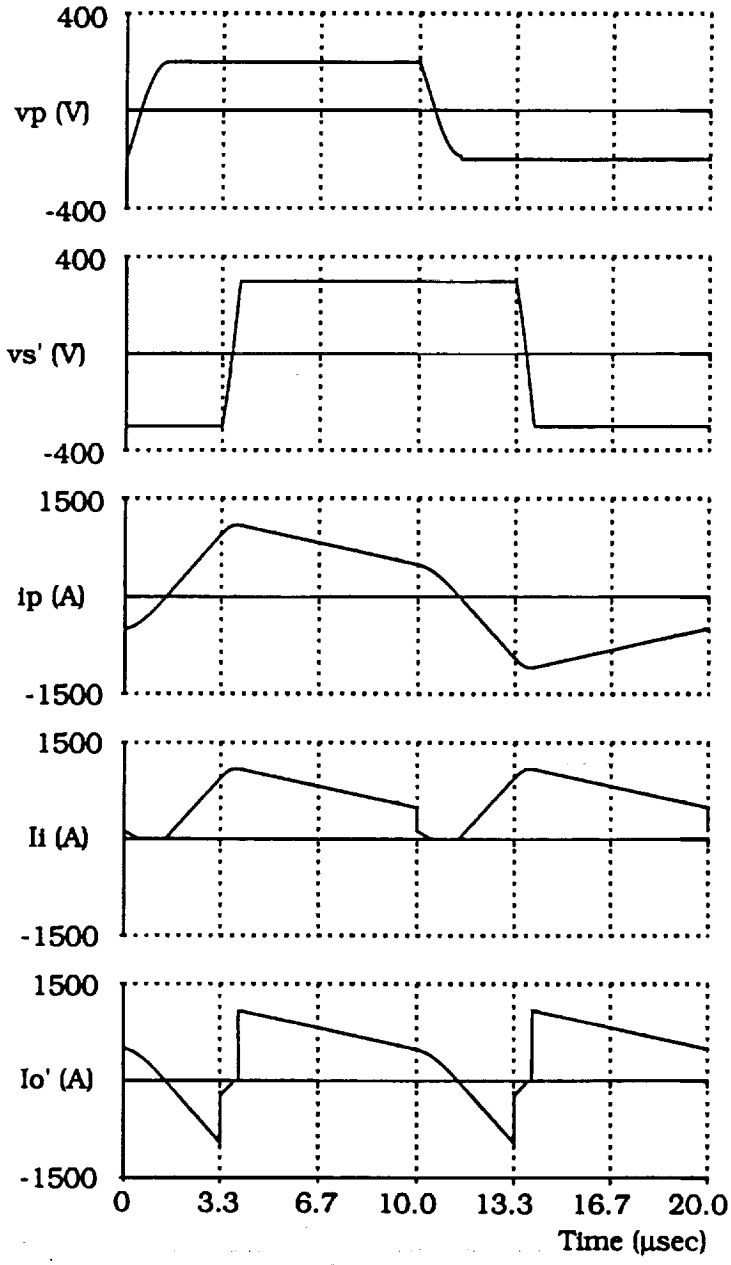

Fig. B.2a Simulated Topology B waveforms in the presence of finite snubber capacitors, with the device(IGBT) turn-off model. d=1.5(boost mode), ϕ=60°, V_I=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V, $C_I = C_O$ = 1μF (input and output snubber capacitors), L = 1μH.

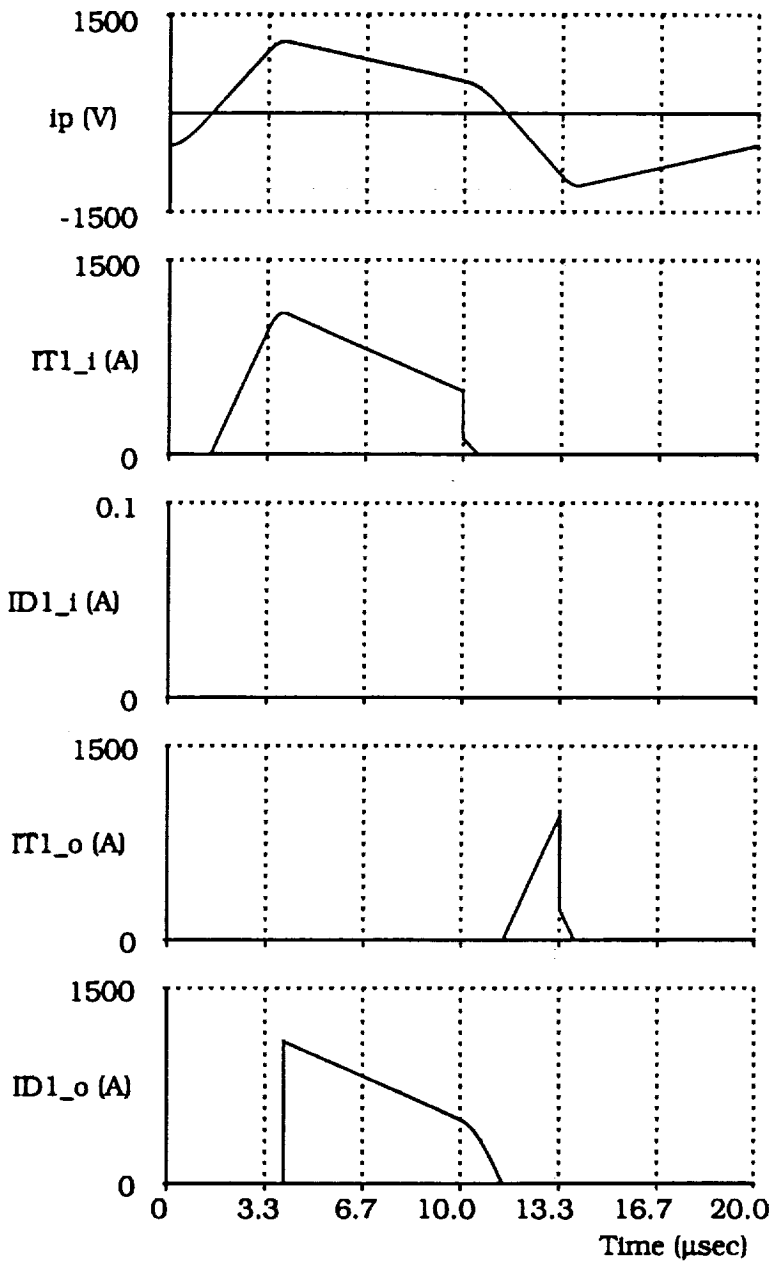

Fig. B.2b Simulated input and output device/diode current waveforms for Topology B, with the device(IGBT) turn-off model. d=1.5(boost mode), $\phi=60°$, V_i=200Vdc, f=50kHz, t_f=0.5μs, K=0.25, V_D=1V, V_T=3V, $C_i = C_o$ = 1μF (input and output snubber capacitors), L = 1μH. Note, the input bridge is operating on its soft-switching boundary indicated by the non-conduction of the diodes.

APPENDIX C

Fourier Series Analysis of the Transformer Primary Current for Topology B

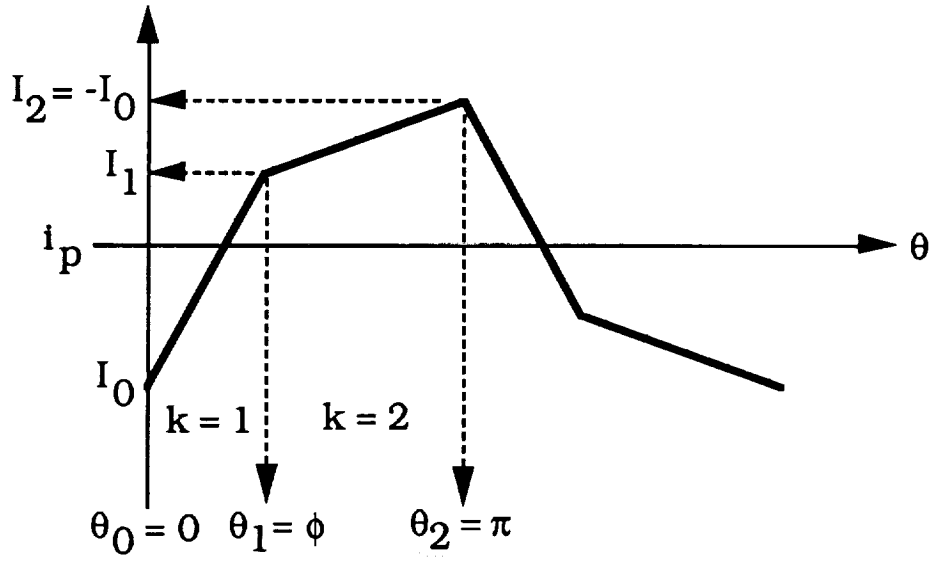

Figure C.1 Typical transformer primary current

Figure C.1 shows a typical waveform for the primary current, $i_p(\theta)$, through the transformer, which is modelled simply by its leakage inductance, for Topology B. In each mode, the segment of the current is linear, and hence can be mathematically expressed, in general, as

$$i_k(\theta) = m_k (\theta - \theta_{k-1}) + c_k \qquad ...(C.1)$$

where, k is the mode no., m_k is the slope of the current segment in the kth mode, given as,

$$m_k = \frac{I_k - I_{k-1}}{\theta_k - \theta_{k-1}} \qquad \text{...(C.2a)}$$

$$c_k = I_{k-1} \qquad \text{...(C.2b)}$$

I_{k-1}, I_k, θ_{k-1} and θ_k are the initial and final values of the current and θ for the kth mode, respectively. The Fourier series coefficients for the above current are given as,

$a_0 = 0$, since the average value is zero.

$$a_n = \frac{2}{\pi}\left[\int_0^{\phi} \{m_1(\theta) + c_1\} \cos(n\theta)\, d\theta + \int_{\phi}^{\pi} \{m_2(\theta - \phi) + c_2\} \cos(n\theta)\, d\theta\right]$$

for n= 1,2... ...(C.3a)

$$b_n = \frac{2}{\pi}\left[\int_0^{\phi}\{m_1(\theta) + c_1\}\sin(n\theta)\,d\theta + \int_{\phi}^{\pi}\{m_2(\theta - \phi) + c_2\}\sin(n\theta)\,d\theta\right]$$

for n= 1,2... ...(C.3b)

where, m_k and c_k are as defined in eqns. (C.2a) and(C.2b).

Substituting for the $m_{k's}$ and c_k's and carrying out the necessary algebra we get,

$$a_n = 0 \qquad \text{for n even}$$

$$a_n = \left[\frac{2}{\pi n^2}\right]\left[\frac{(I_1 - I_0)\cos(n\phi - 1)}{\phi} + \frac{(I_1 + I_0)\cos(n\phi + 1)}{(\pi - \phi)}\right]$$

for n odd ...(C.4)

Now, from eqns. (3.3.5) and (3.3.6) (Chapter 3)

$$I_0 = -\frac{V_i}{2\omega L}\left[2d\phi + \pi(1 - d)\right] \qquad ...(C.5a)$$

and,

$$I_1 = \frac{V_i}{2\omega L}\left[2\phi - \pi(1 - d)\right] \qquad ...(C.5b)$$

Substituting the values of I_0 and I_1 from eqns. (C.5a) and (C.5b) into eqn. (C.4) and simplifying, we get,

$$a_n = \frac{4V_i}{\pi\omega L n^2}\left[d\cos(n\phi) - 1\right] \qquad \ldots(C.6)$$

Similarly,

$$b_n = 0 \qquad \text{for n even}$$

$$b_n = \frac{4V_i}{\pi\omega L n^2}\left[d\sin(n\phi)\right] \qquad \text{for n odd} \qquad \ldots(C.7)$$

The amplitude of the nth odd harmonic can now be expressed as,

$$c_n = \sqrt{a_n^2 + b_n^2} = \frac{4V_i}{\pi\omega L n^2}\sqrt{d^2 - 2d\cos(\quad) + 1} \qquad \ldots(C.8)$$

For d = 1, we get from eqn. (C.8),

$$c_n = \frac{8V_i}{\pi\omega L n^2}\sin\left(\frac{n\phi}{2}\right) \qquad n = 1, 3, 5\ldots \qquad \ldots(C.9)$$

Figure C.2 shows the variation of the first four significant harmonics with ϕ, over the range 0 to $\pi/2$, for d = 1.

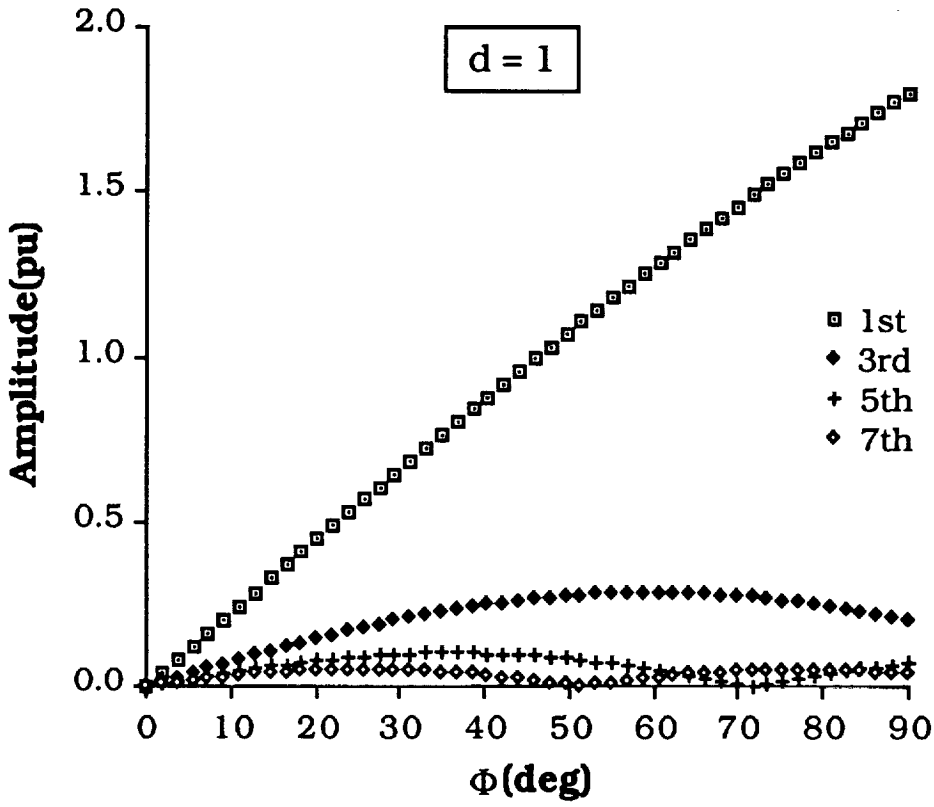

Figure C.2 Current harmonic amplitudes as a function of ϕ. The amplitudes are normalized to the current base, $I_b = V_i/\omega L$.

APPENDIX D

Demonstration of usage of "TID"

TRANSFORMER AND INDUCTOR WINDING DESIGN - VERSION 1A

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AUTHOR - Braham Ferreira

Output Control :

Total Power Dissipation

Effective Resistance

Power Dissipation Density Plot

Magnetic Field Intensity Plot

SUB-MENU FOR GENERAL CONFIGURATION

Magnetic Core Parameters :

Permeability (relative to air) of core = 2500

Diameter of Center Leg of Core = 0.07497m

Closed Window Ratio (percentage) = 52.00

Open Window Ratio (percentage) = 48.00

Airgaps (Number = 0.1 or 2) = 0

Window Dimensions :

Height of Window = 0.01166m

Width of Window = 0.15814m

Frequency Components :

First Harmonic = 50000.0

C-4

Quantity of frequency components (maximum of 9) = 3

SUB-MENU FOR WINDING CONFIGURATION

Number of winding sections = 2

Winding Sections

1: Bottom co-ordinates = (0.0013, 0.0013)

Top co-ordinates = (0.1569, 0.0032)

Turns = (1x3)

Type : COPPER, Monofilar, Strip (0.00051m, 0.15560m)

Current = (430.300, 109.200, 32.700) A

2: Bottom co-ordinates = (0.0345, 0.0044)

Top co-ordinates = (0.1236, 0.0104)

Turns = (15x1)

Type : COPPER, Monofilar, Litz (0.00582m, 0.00013m, 1050)

Current = (-86.100, -21.800, -6.500) A

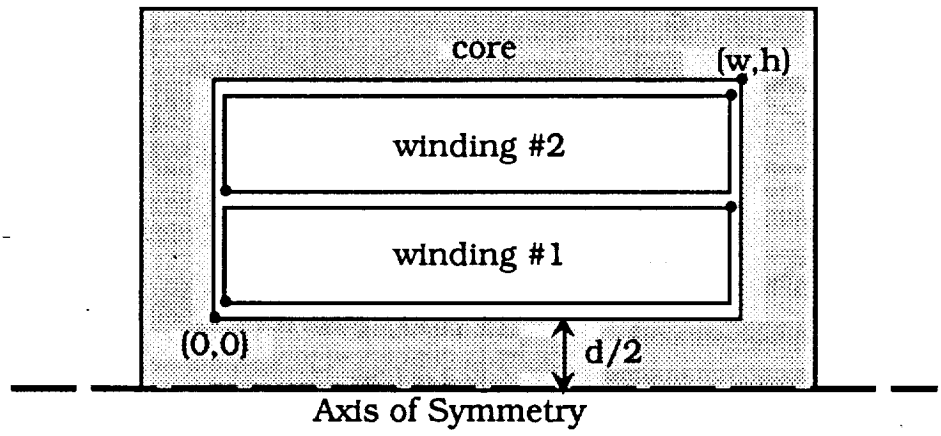

Figure D.1 Winding arrangement X

APPENDIX E

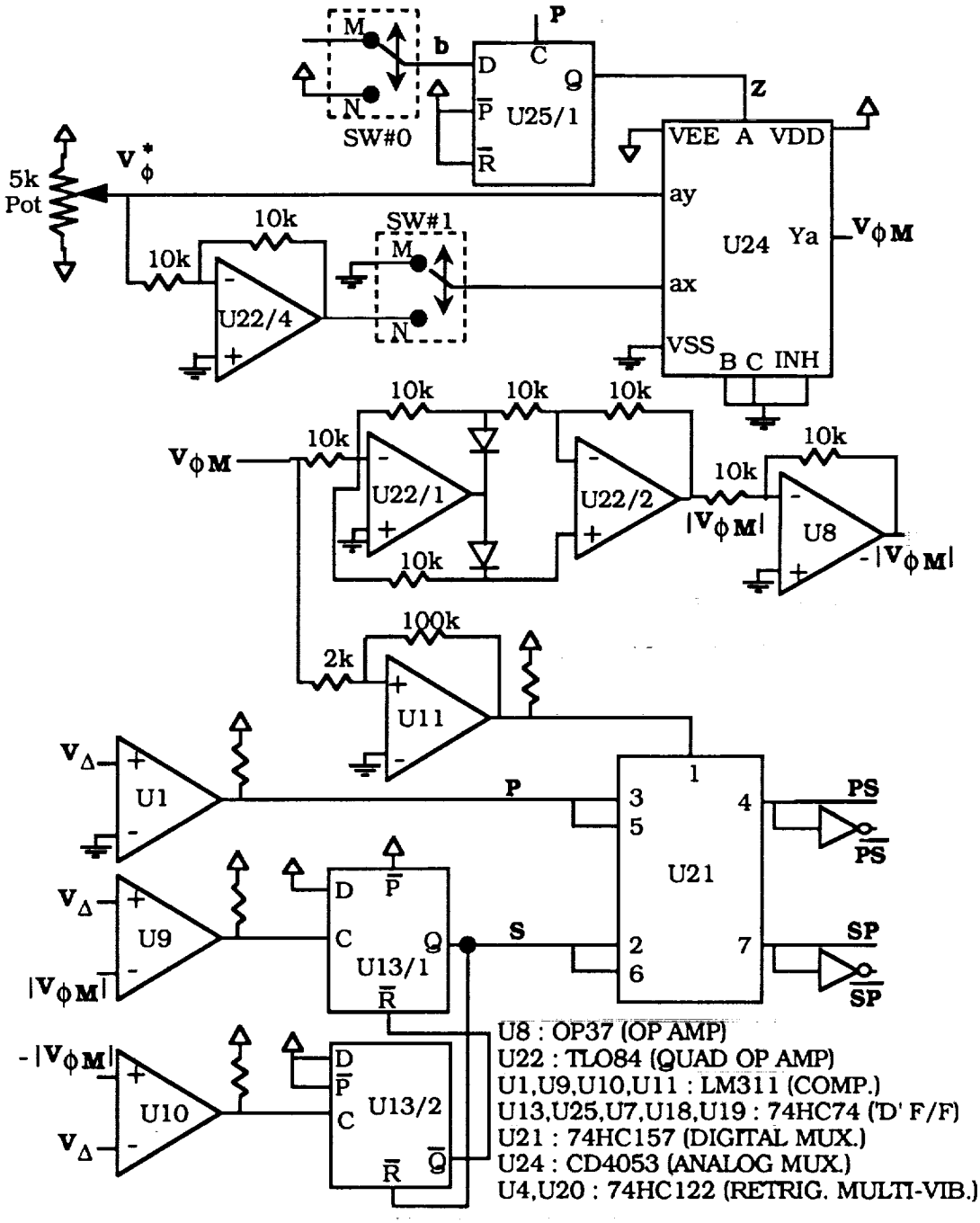

Fig. E.1 Circuit schematic of open loop phase-shift controller, contd...

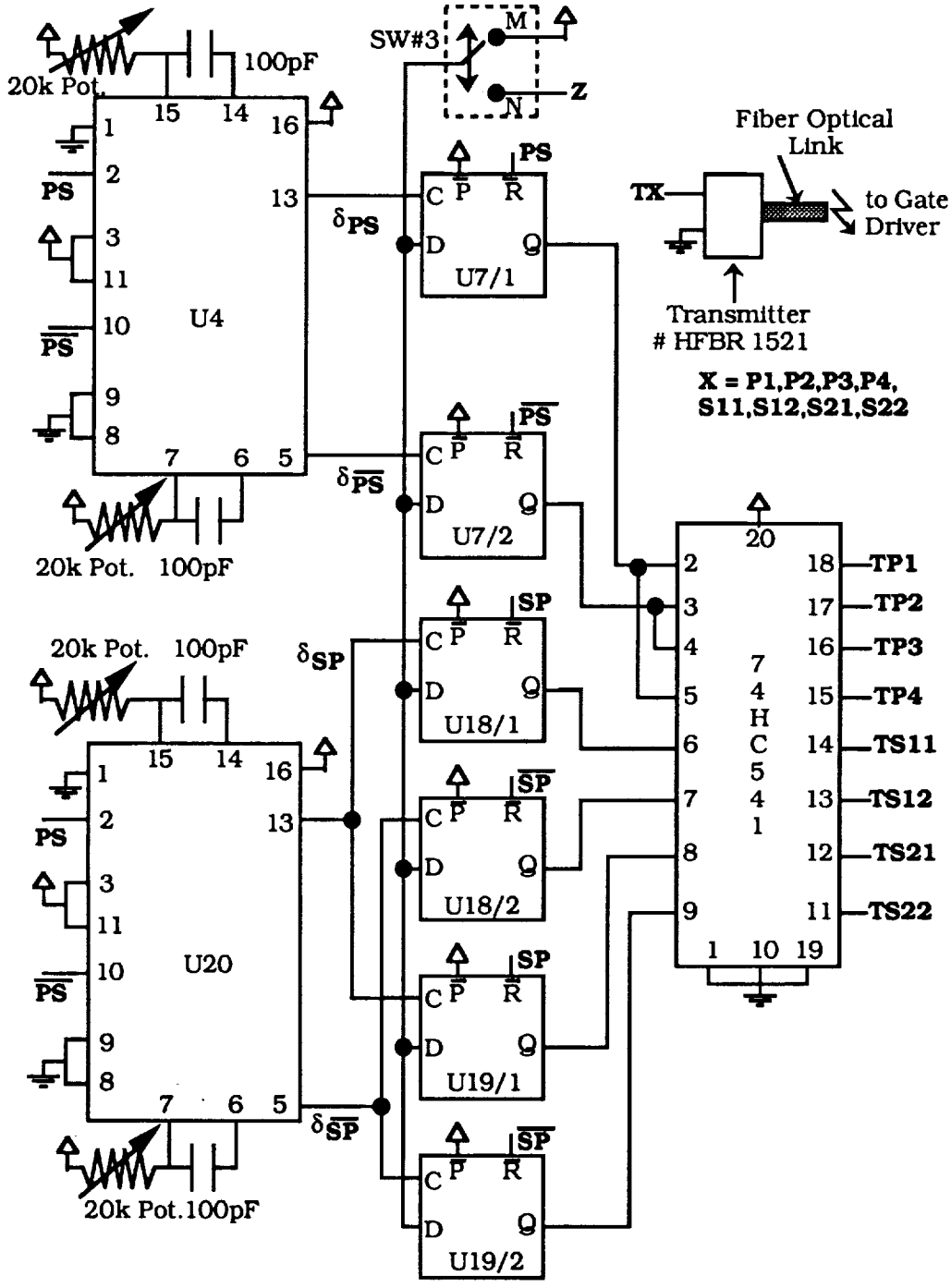

Fig. E.1 Circuit schematic of open loop phase-shift controller.

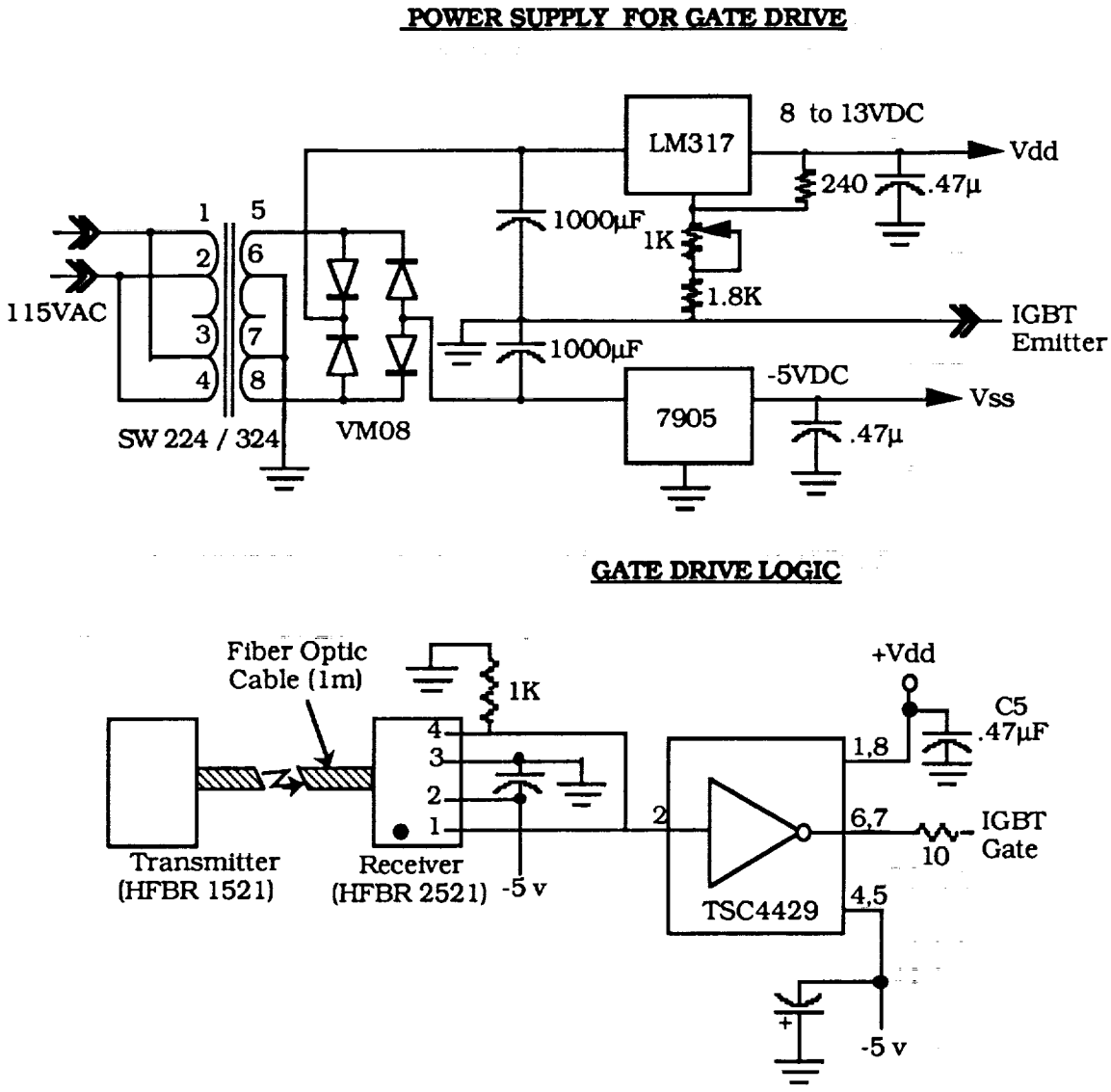

Fig. E.2 Circuit schematic of Gate driver card for IGBTs.

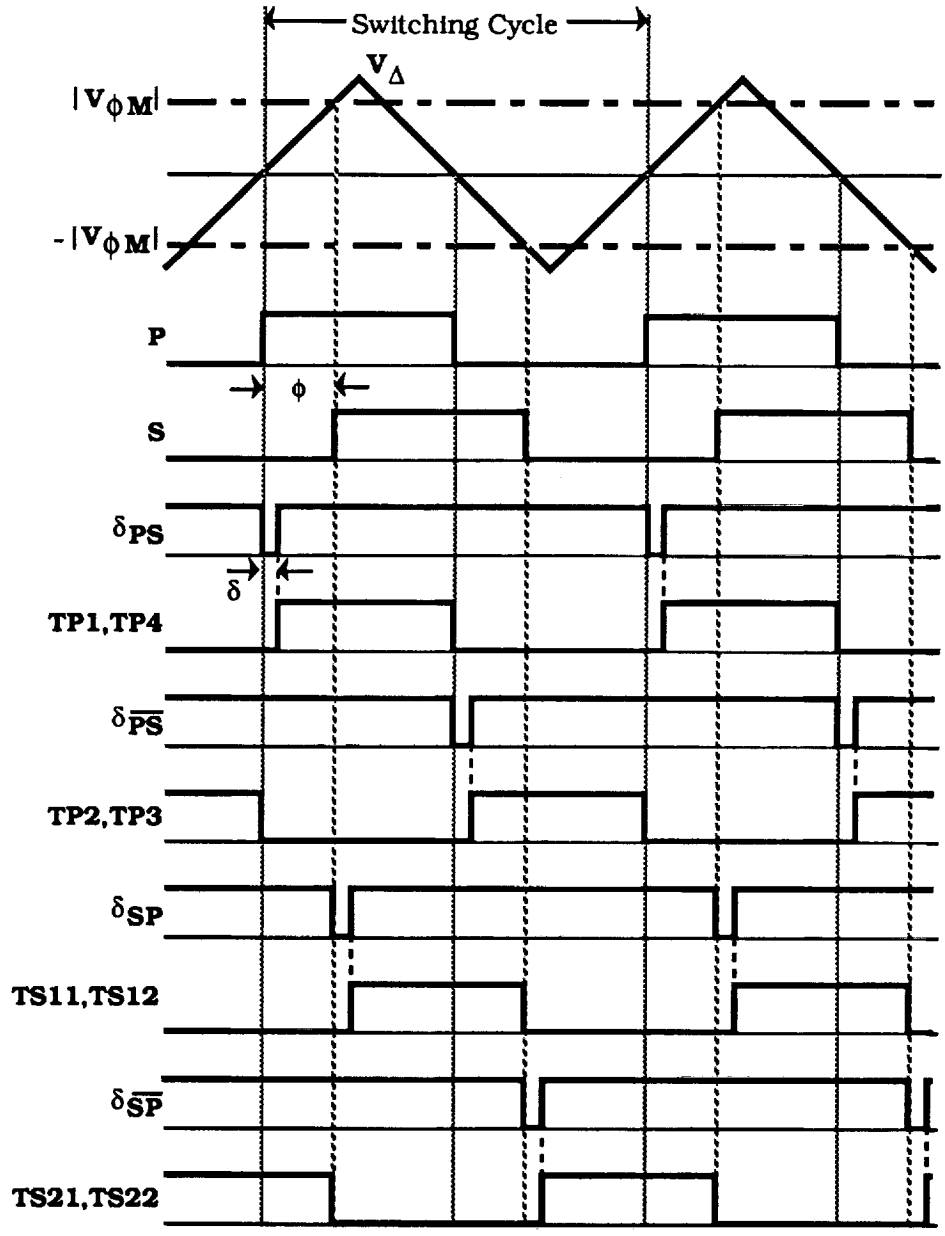

Fig. E.3 Relevant controller and gating signals. (See Fig. E.1)
δ = dead time between complementary switches.
ϕ = Control phase-shift.

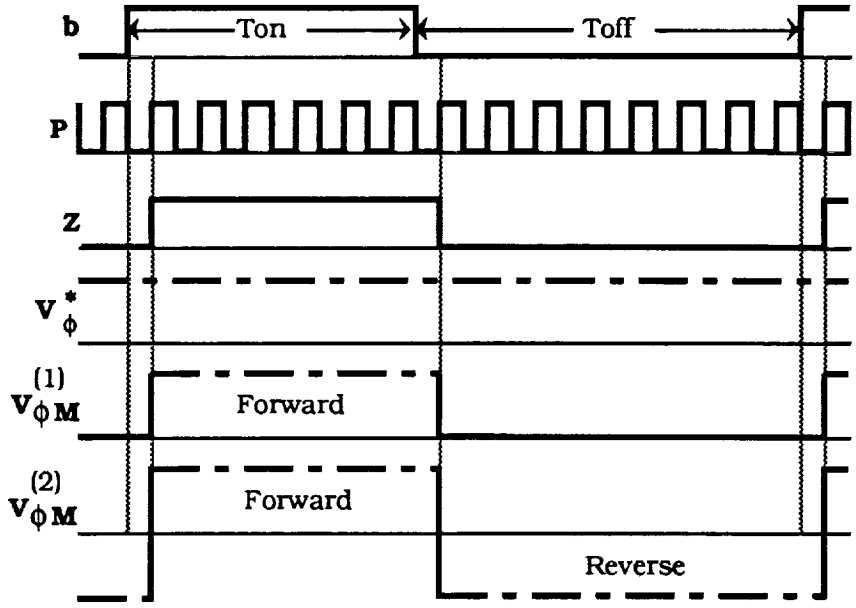

Fig. E.4 Relevant controller signals for various modes of operation. (See Fig. E.1, Table E.1)

Table E.1
(COMBINATION OF SWITCHES ON THE CONTROLLER FOR DIFFERENT MODES OF OPERATION)

Mode of Power Transfer	SW #0	SW #1	SW #2	Remarks
Open Loop Forward Continuous	N	N	M	$0 \le V_\phi^* < V_{\Delta pk}$
Open Loop Forward Pulsed	M	N	N	$0 \le V_\phi^* < V_{\Delta pk}$
Open Loop Reverse Continuous	N	M	M	$0 \ge V_\phi^* > -V_{\Delta pk}$
Open Loop Reverse Pulsed	M	M	N	$0 \ge V_\phi^* > -V_{\Delta pk}$
Open Loop Bi-directional	M	M	M	$0 \le V_\phi^* < V_{\Delta pk}$

A Three-Phase Soft-Switched High-Power-Density dc/dc Converter for High-Power Applications

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Abstract—**Three dc/dc converter topologies suitable for high-power-density high-power applications are presented. All three circuits operate in a soft-switched manner, making possible a reduction in device switching losses and an increase in switching frequency. The three-phase dual-bridge converter proposed is seen to have the most favorable characteristics. This converter consists of two three-phase inverter stages operating in a high-frequency six-step mode. In contrast to existing single-phase ac-link dc/dc converters, lower turn-off peak currents in the power devices and lower rms current ratings for both the input and output filter capacitors are obtained. This is in addition to smaller filter element values due to the higher-frequency content of the input and output waveforms. Furthermore, the use of a three-phase symmetrical transformer instead of single-phase transformers and a better utilization of the available apparent power of the transformer (as a consequence of the controlled output inverter) significantly increase the power density attainable.**

Introduction

THE AREA of high-power-density dc/dc converters has been an important research topic, especially for switched-mode power-supply applications rated at up to 500 W. The needs of the next generation of aerospace applications require extremely high-power densities at power levels in the multikilowatt to megawatt range. The implications of realizing high-power density and low-weight systems at these power levels have rarely been addressed. This paper examines considerations for the selection of topologies that can realize the low-weight constraints that are of primary importance.

Recognizing that higher switching frequencies are the key to reducing the size of the transformer and filter elements, it is apparent that some form of soft-switching converter with zero-switching loss is required if system efficiencies and heat sink size are to be maintained at a reasonable level. By far the most attractive circuit so far has been the series resonant converter (SRC) [1]. Using thyristors with a single LC circuit for device commutation and energy transfer, the topology is extremely simple in realization and offers the possibility of power densities in the 0.9–1.0 kg/kW range at power levels up to 100 kW.

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IEEE Log Number 9040502.

The following problems can be identified with the SRC. Thyristor commutation requirements demand higher current ratings from the devices and higher VA ratings from the LC components. Thyristor recovery times significantly slow down the maximum switching frequencies attainable. Snubber inductors and RC networks are needed to effect current transfer without encountering a diode recovery problem. Capacitive input and output filters have to handle ripple currents at least as large as the load current. Although switching frequencies in the 10-kHz range yield dramatic reduction in converter size when compared to conventional hard-switching circuits, it is clear that systems operating at similar frequencies and with lower component ratings are potentially capable of even higher power densities.

This paper proposes a new soft-switching dc/dc converter topology suitable for high-power applications. Soft-switched converters are characterized by intrinsic modes of operation that allow an automatic and lossless resetting of the snubber elements through an appropriate recirculation of trapped energy. The capability to eliminate losses associated with the snubber now permit the use of oversized snubbers resulting in dramatically lower device-switching losses, even at substantially higher frequencies. Examples of soft-switched dc/dc converters are the parallel output SRC operated above resonance [2], the pseudo-resonant converter, the resonant pole [3], [4], and all quasi-resonant converters [5]–[7]. For multiquadrant operation and for dc/ac inverter applications, typical examples of soft-switched topologies are the resonant dc/link inverter and the quasi-resonant current mode or resonant pole inverter [8]. The proposed circuit utilizes the resonant pole as the basic switching element for both input and output devices and yields substantial benefits in power density and operating characteristics.

Soft-Switched DC/DC Converters

The preferred dc/dc converter topology for high-power applications has been the full-bridge circuit operated at constant frequency under a pulsewidth control strategy. The topology features minimal voltage and current stresses in the devices, minimum VA rating of the high frequency transformer, as well as low ripple current levels in the output filter capacitor. The power density levels that can be reached are limited by peak and average device-switching losses, transformer leakage inductances, and output rectifier reverse recovery. The factors above constrain the maximum frequency attainable, and thus the smallest size possible, given the state of the art in component technology. Most of the resonant converters reported in literature

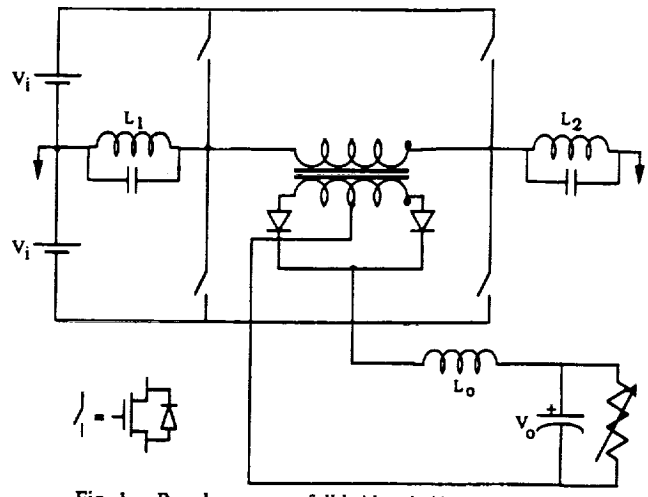


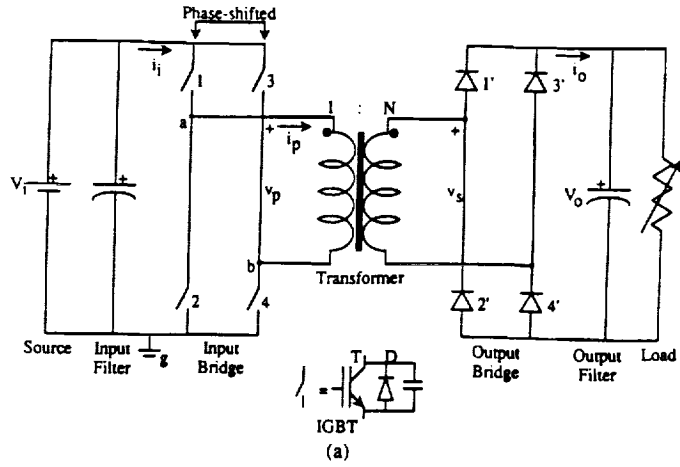
Fig. 1. Pseudo-resonant full bridge dc/dc converter [3].

attempt to tackle one or more of the problems listed, typically at the expense of substantially higher component stresses [5]–[7]. For high-power operation, that is unacceptable. Soft-switching variations of the full-bridge converter are thus the most favored topologies.

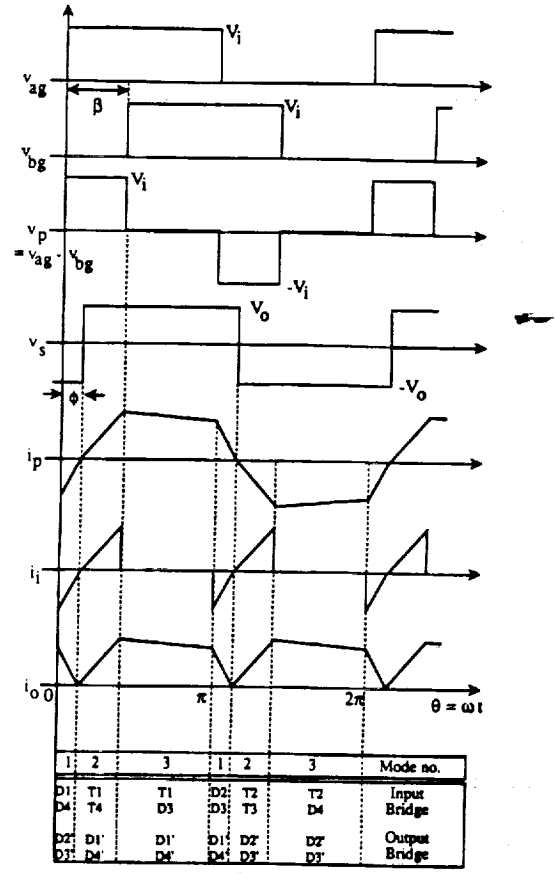
The pseudo-resonant dc/dc converter proposed in [3] is shown in Fig. 1. It uses capacitive snubbers and can be designed with device stresses approaching that of the conventional full bridge. However, the circuit uses the transformer as a voltage transfer element, and the interactions of its leakage inductance (L_{lk}) and the output rectifier are unresolved. The maximum switching-frequency limit is reached when the energy lost due to L_{lk} and the peak-diode reverse-recovery current become unacceptable.

Transferring the output filter inductance to the ac side completely changes the operating characteristics of the circuit [3]. As shown in Fig. 2(a), the inductance L_o is now in series with the transformer leakage inductance L_{lk}. Further, energy trapped in ($L_{lk} + L_o$) during reverse recovery is now transferred to the load in a lossless manner. This implies that a further increase in switching frequency may be possible. It can also be shown that the additional inductors L_1 and L_2 required in the previous circuit (Fig. 1) are no longer absolutely essential, since adequate control range can be obtained at constant frequency while maintaining soft switching for all devices. Operating waveforms for this single-phase phase-shifted dc/dc converter (Topology A) are shown in Fig. 2(b). It can be seen that soft switching is obtained by ensuring that device turn-on only occurs when its antiparallel diode is conducting. The biggest problem with this circuit seems to be the high ripple current in the output filter capacitor. For low-voltage high-current power supplies, this is a very important consideration. For high-power high-voltage aerospace applications, it is not seen to be a major problem because power densities obtainable with multilayer ceramic capacitors are at least as good as with inductors.

It has been proposed in [9] that the diode recovery process is akin to the existence of an active device in antiparallel with it. Observing that the circuit in Fig. 2(a) naturally handles the diode reverse recovery process, it is proposed that the diodes be replaced by active devices as shown in Fig. 3(a) [10]. Many high-frequency converters already use synchronous rectifiers in essentially the same location. The converter can now be operated with a simpler control strategy in which the input and output bridges generate square waves that are phase shifted from each other. In keeping with our philosophy, regions of operation can



(a)

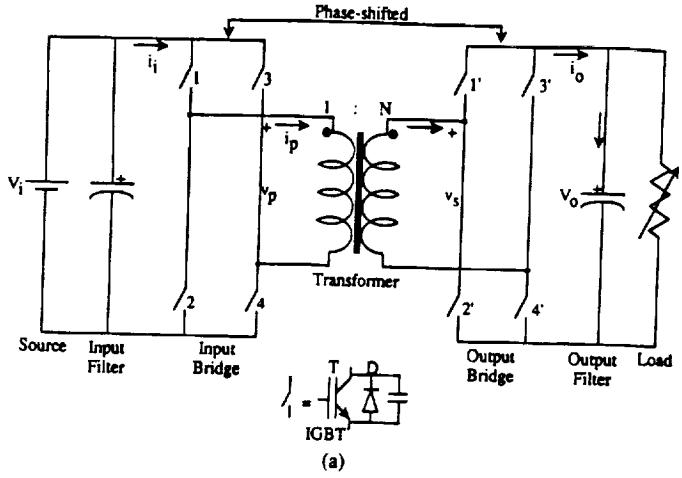


(b)

Fig. 2. (a) Single-phase phase-shifted dc/dc converter, Topology A; (b) idealized operating waveforms for topology A.

be identified that permit soft switching of all devices in both bridges. Fig. 3(b) shows operating waveforms for the single-phase dual-bridge dc/dc converter topology (Topology B).

The circuit in Fig. 3(a) can be extended to a polyphase version. The three-phase dual-bridge circuit (Topology C) is shown in Fig. 4(a). Again, examining the modes of operation for the converter, it is possible to identify regions where both sets of switches experience soft switching. As in the case of the single-phase dual-active bridge converter, both bridges generate quasi-square-waves phase shifted from each other. It should be noted that the soft-switching transition is actually resonant in nature [3], [8] but is assumed to be almost instantaneous for the derivation of first-order operating characteristics. The three-phase dual-active bridge converter has substantially lower filter



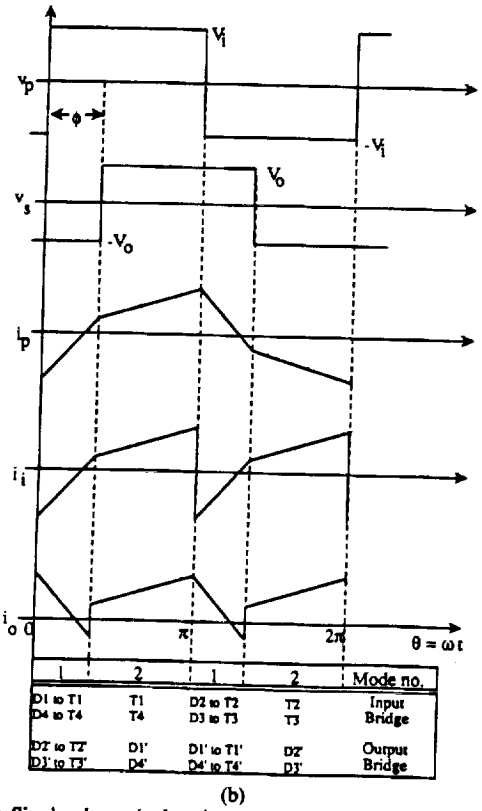
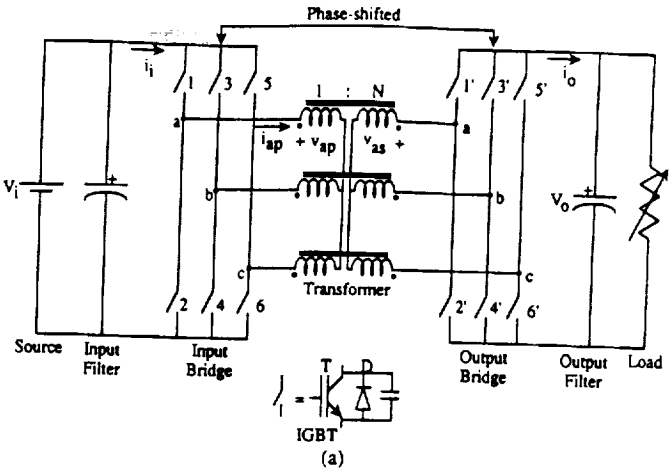


Fig. 3. (a) Single-phase dual active bridge dc/dc converter, Topology B; (b) idealized operating waveforms for topology B.



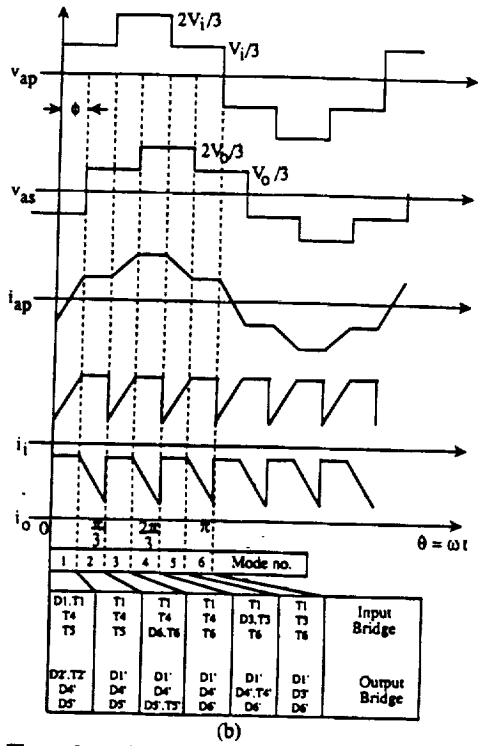


Fig. 4. (a) Three-phase dual active bridge dc/dc converter, Topology C; (b) idealized operating waveforms for topology C.

ratings when compared to its single-phase counterpart. Consequently, it has the potential of realizing the highest power density.

It should be noted that all three converters, denoted Topology A, B, and C for circuits in Figs. 2, 3, and 4, respectively, exhibit desirable properties with regard to parasitics such as device storage time, transformer leakage inductance, and diode reverse recovery. It is shown in the paper that transformers, which use the leakage impedance as an energy transfer element, have the potential of reaching higher power densities. Although this technique has been used extensively at lower power levels, it has been felt that the higher VA rating of the composite transformer was an unacceptable penalty at higher power levels. It will be shown that the resulting increase in switching frequency more than compensates for the increased VA rating, allowing substantial reduction in the overall size of the converter. The use of dual-active bridges also yields unexpected gains in power density; as will be shown, and permits bidirectional power flow. Analysis in the paper is restricted to unidirectional power flow only.

Analysis of the Single-Phase Converters

Topology A

In order to derive the operating characteristics of the three dc/dc converters, it is assumed that the transfer of current from device to diode on turn-off is instantaneous. The actual switching locus depends on the value of snubber capacitance C used and the current level. For a typical device such as a bipolar junction transistor (BJT) with a current fall time t_f and a turn-off current I_m, the device energy loss per switching cycle can be found approximately to be [11]

$$E_{sw} = \frac{I_m^2 t_f^2}{24C}. \tag{1}$$

Since there are no turn-on or snubber dump losses, C can be

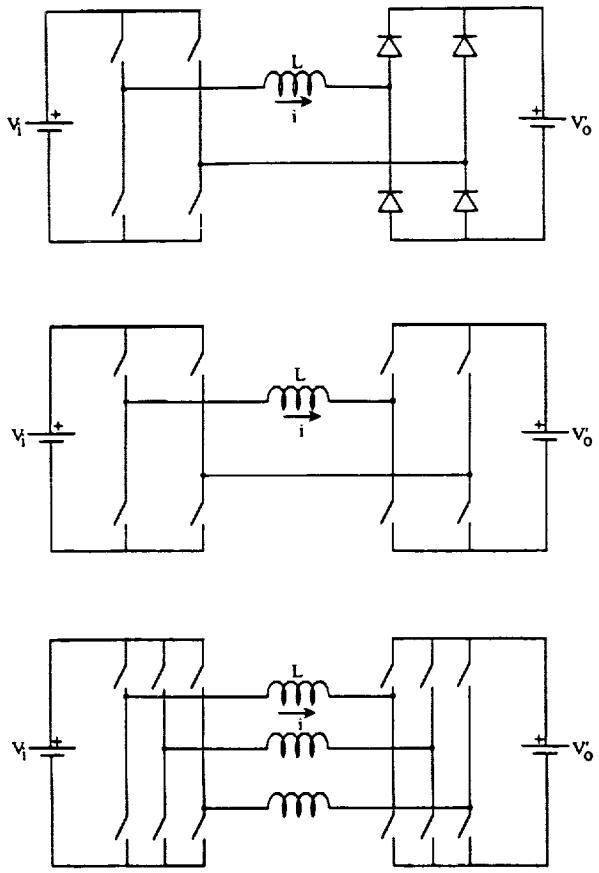


Fig. 5. Primary referred equivalent circuits for the three topologies A, B, and C.

made fairly small while retaining a fast-switching characteristic and low-device losses, simultaneously. This justifies the assumption of a fast, almost instantaneous switching transition for analysis over a full cycle.

The primary-referred equivalent circuits for the three converters are shown in Fig. 5. Replacing the transformer with a leakage inductance L simplifies circuit analysis. For Topology A, three operating modes can be identified as shown in Fig. 2(b). The phase shift between the two bridges is ϕ, dependent on L and the load. The equivalent voltage applied across the load is V_{ab} and has pulsewidth β, where β is the controlled phase shift between the two resonant poles of the input bridge. The inductor current i as a function of $\theta = \omega t$, where ω is the switching frequency, is as follows. In Mode 1,

$$i(\theta) = \left[\frac{V_i + V_o'}{\omega L}\right]\theta + i(0) \tag{2}$$

where V_i, V_o' are input and primary-referred output dc voltages and $i(0)$ is the initial current at $\theta = 0$. Mode 1 ends at $\theta = \phi$. In Mode 2,

$$i(\theta) = \left[\frac{V_i - V_o'}{\omega L}\right](\theta - \phi) + i(\phi). \tag{3}$$

Similarly, the current in Mode 3 can be found to be

$$i(\theta) = \left[\frac{-V_o'}{\omega L}\right](\theta - \beta) + i(\beta). \tag{4}$$

At the end of the half cycle $i(\pi) = -i(0)$. Solving for $i(0)$, we can obtain the complete current waveform. The soft-switching constraints require that the device be conducting at turn-off. From Fig. 2(b) this implies that $i(\pi) \geq 0$. Further, given the output rectifier it is clear that $i(\phi) = 0$. Using the preceding relationships,

$$\phi = \frac{1}{2}(\beta - d\pi). \tag{5}$$

In addition, since $\phi \geq 0$, we get

$$\beta - d\pi \geq 0 \tag{6}$$

where

$$d = \frac{V_o'}{V_i}. \tag{7}$$

The parameter d represents the primary-referred dc voltage gain of the converter, often referred to as the dc conversion ratio. From $i(\theta)$ and the converter switching functions, the supply or output average current can be found to yield power transfer at a given β, d, and ω. This is found to be

$$P_o = V_i I_i = \frac{dV_i^2}{4\omega L}\left[2\beta - \pi d^2 - \frac{\beta^2}{\pi}\right] \tag{8}$$

where I_i is the average value of $i(\theta)$. Input and output filter-capacitor rms current ratings can also be calculated from $i(\theta)$. Peak device voltage and current ratings are also easily found. The kVA rating of the transformer is calculated as

$$(\text{kVA})_T = \frac{1}{2}\left[v_{\text{pri(rms)}} i_{\text{pri(rms)}} + v_{\text{sec(rms)}} i_{\text{sec(rms)}}\right], \tag{9}$$

which can be derived as (neglecting magnetizing current)

$$(\text{kVA})_T = V_i\left[\sqrt{\frac{\beta}{\pi}} + d\right] I_{\text{rms}} \tag{10}$$

where I_{rms} is the rms value of $i(\theta)$. Operating characteristics for Topology A are calculated based on the principles listed previously and are shown in Fig. 6. All quantities have been normalized to the following base:

$$\text{voltage base } V_b = V_i$$

$$\text{current base } I_b = \frac{V_i}{\omega L}$$

$$\text{power base } P_b = V_b I_b = \frac{V_i^2}{\omega L}. \tag{11}$$

Fig. 6(a) depicts the range of control possible with variation of β while maintaining soft-switching operation for all four input devices. For each value of d the output power is shown over the soft-switching region. The locus of the minimum power for each d defines the soft-switching boundary corresponding to $\beta = d\pi$. It is seen that maximum power transfer occurs at $\beta = 180°$ and $d = 0.58$. Fig. 6(b) shows a variation of the transformer kVA versus the power output P_o. It is seen that at the design point (maximum power transfer), the $P_o/(\text{kVA})_T$ ratio is approximately 0.64 pu.

Topology B

A similar analysis can be carried out for Topology B. This converter has only two modes of operation. The two bridges are presumed to operate with controlled phase shift ϕ. The current $i(\theta)$ is once again given by (2) and (3) for Modes 1 and 2.

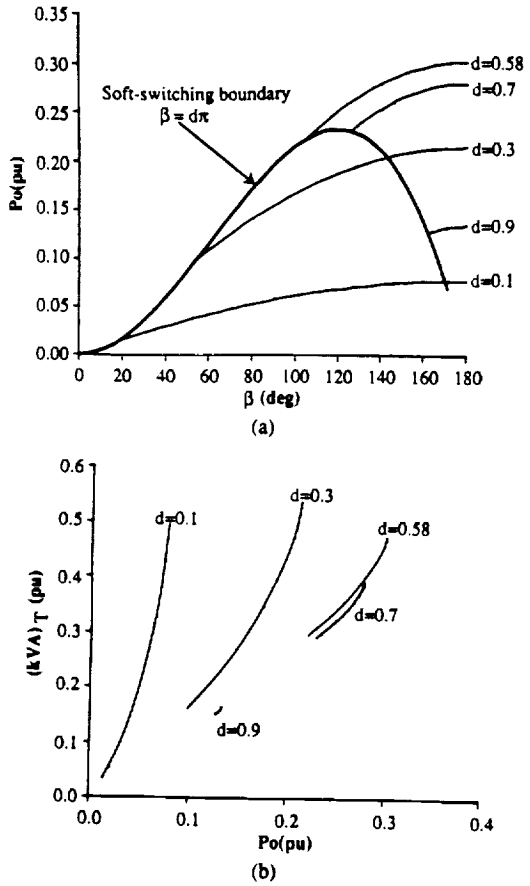


Fig. 6. (a) Output power versus β, with d as parameter for topology A; (b) transformer kVA versus output power, with d as parameter for topology A.

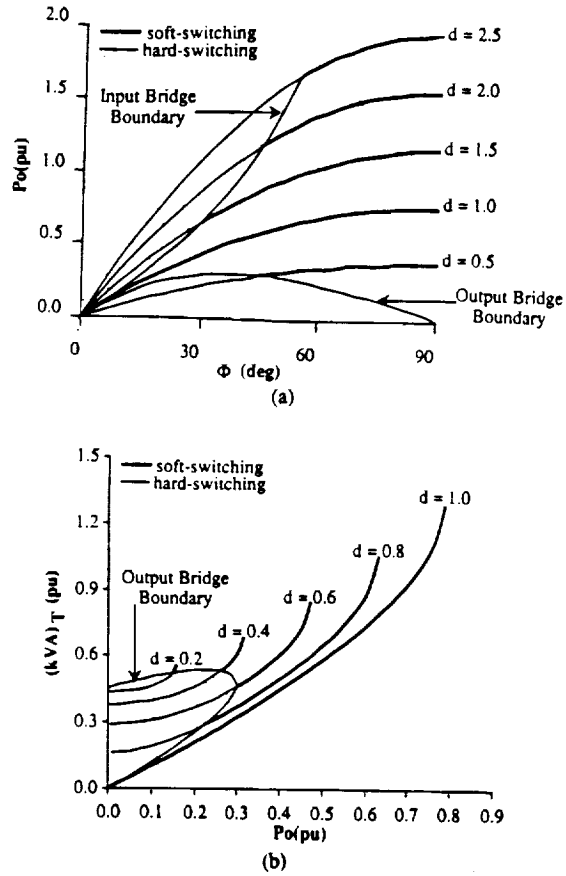


Fig. 7. (a) Output power versus ϕ, with d as parameter for topology B; (b) transformer kVA versus output power, with d as parameter for topology B.

respectively. The boundary conditions now dictate that $i(0) = -i(\pi)$ at the end of Mode 2. Solving for $i(\theta)$, the output power P_o and transformer kVA are given as

$$P_0 = \frac{V_i^2}{\omega L} d\phi\left[1 - \frac{\phi}{\pi}\right] \tag{12}$$

$$(\text{kVA})_T = V_1[1 + d]\, I_{\text{rms}}. \tag{13}$$

The constraints, which define soft-switching boundaries, can now be specified for the input and output bridges to be $i(0) \leq 0$ and $i(\phi) \geq 0$, respectively. These constraints enclose the desired operating region for the converter. Exceeding the first constraint results in natural commutation of the input bridge devices and gives snubber dump. For the output bridge, the constraint equation corresponds to diode bridge operation.

Fig. 7(a) shows the variation of normalized P_o as a function of ϕ for different values of d. The input bridge and output bridge boundaries enclosing the soft-switching region are shown. For $d = 1$ it can be seen that ϕ can vary over the entire range of 0–90°, giving control from zero to full power. The curves corresponding to $d > 1$ represent boost operation.

Fig. 7(b) plots the transformer kVA against the output power for various values of d. The output bridge boundary, corresponding to the output diode bridge, is identical to that in Fig. 6(b) (for Topology A) with $\beta = \pi$. An interesting feature of Topology B can be brought to light by examining the minimum transformer kVA (0.475 pu) required for transferring the maximum output power (0.302 pu) on the diode bridge boundary. For the same kVA the output power can be increased to 0.422 pu at $d = 1$ with dual-active bridges. This gives us a transformer utilization (defined as $P_o/(\text{kVA})_T$) of 0.89, an improvement of 40%.

Compared to normal hard-switched converters with $P_o/(\text{kVA})_T$ ratios approaching unity, this may seem to be very poor transformer utilization. However, if the switching frequency for the proposed converter can be made substantially higher, actual size/weight could be much lower. Transformer sizing will be examined in greater detail later in the paper. It is apparent that along with further gains in transformer power density, a significant reduction in input/output filter size and ripple current rating will result from selecting the three-phase dc/dc dual-bridge converter.

Analysis of the Three-Phase dc/dc Converter

The circuit schematic of the new three-phase dual-bridge soft-switching ac-link dc/dc converter is shown in Fig. 4. The proposed converter consists of two three-phase inverter stages, each operating in a six-step mode with controlled phase shift. Using two active bridges not only permits bidirectional power flow, but also allows control at a fixed frequency. The ac-link transformer is Y–Y-connected and is three-phase symmetric with the leakage inductances used as energy transfer elements.

In the following analysis, it is assumed that the primary and secondary resistances of the transformer can be neglected and the turns ratio is 1:1. Fig. 8 shows the schematic of the three-phase symmetric transformer. Using the relationship $i_a + i_b + i_c = 0$ for Y-connected transformers, the transformer equa-

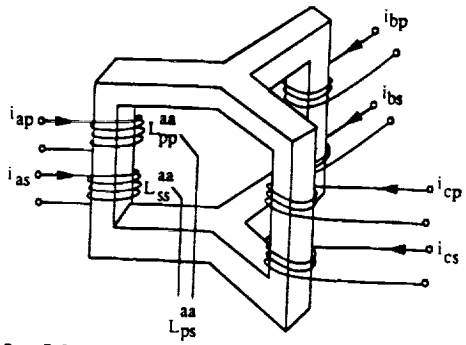


Fig. 8. Schematic of a symmetrical three-phase transformer.

tions can be derived to be

$$V_{ap}(t) = L_{pl}\frac{di_{ap}}{dt} + \left[L_{pp}^{aa} + L_{pp}^{ab}\right]\frac{di_{ap}}{dt} + \left[L_{ps}^{aa} + L_{ps}^{ab}\right]\frac{di_{as}}{dt} \quad (14)$$

and

$$V_{as}(t) = L_{sl}\frac{di_{as}}{dt} + \left[L_{ss}^{aa} + L_{ss}^{ab}\right]\frac{di_{as}}{dt} + \left[L_{sp}^{aa} + L_{sp}^{ab}\right]\frac{di_{ap}}{dt} \quad (15)$$

where V_{ap} and V_{as} are the primary and secondary voltages for the a-phase, L_{pl} and L_{sl} the primary and secondary leakage inductances, L_{pp} and L_{ss} are self-inductances, and L_{ps} and L_{sp} are the mutual inductances between the appropriate phase windings given by the superscript notation used.

Using properties of a symmetric transformer and defining

$$L_m = L_{ss}^{aa} + L_{ss}^{ab} = L_{pp}^{aa} + L_{pp}^{ab}, \quad (16)$$

one can derive

$$\sigma(L_m + L_{sl})\frac{di_{as}}{dt} = V_{as}(t) - \frac{L_m}{L_m + L_{pl}}V_{ap}(t) \quad (17)$$

$$\sigma(L_m + L_{pl})\frac{di_{ap}}{dt} = V_{ap}(t) - \frac{L_m}{L_m + L_{sl}}V_{as}(t) \quad (18)$$

where σ is a leakage factor given by

$$\sigma = \frac{(L_m + L_{sl})(L_m + L_{pl}) - L_m^2}{(L_m + L_{pl})(L_m + L_{sl})}. \quad (19)$$

The value of σ is typically a small number around the ratio of the leakage to the magnetizing inductance.

Equations (17) and (18) are the basic equations that govern the current in the circuit. Further assuming that $L_{sl} = L_{pl} \ll L_m$ (for 1:1 turns ratio), then (17) and (18) reduce to

$$L_\sigma\frac{di_{as}}{dt} = V_{as}(t) - V_{ap}(t) \quad (20)$$

$$L_\sigma\frac{di_{ap}}{dt} = V_{ap}(t) - V_{as}(t) \quad (21)$$

where

$$L_\sigma = \sigma(L_m + L_{sl}) = \sigma(L_m + L_{pl}) = (L_{sl} + L_{pl}). \quad (22)$$

The simplified single equivalent circuit reduces to that shown in Fig. 5(c) with $L = L_\sigma$. It can be seen that with the preceding assumptions, $i_{as} = i_{ap} = i(\theta)$.

In order to calculate the three line currents, the classic six-step line-to-neutral voltage waveform is assumed for both the primary and secondary windings. The difference between the two voltages is applied across L. Six modes, corresponding to different driving voltages, can be identified over a 180° conduction cycle. Using the property of a balanced three-phase set and $i_a + i_b + i_c = 0$, one can obtain full information by calculating two currents over 1/3 of a period. Solving for $i(\theta)$ over a half period 0 to π,

for $0 \le \theta \le \phi$

$$i(\theta) = i(0) + \frac{V_i(1 + d)}{3\omega L}\theta \quad (23)$$

for $\phi \le \theta \le \pi/3$

$$i(\theta) = i(\phi) + \frac{V_i(1 - d)}{3\omega L}(\theta - \phi) \quad (24)$$

for $\pi/3 \le \theta \le \phi + \pi/3$

$$i(\theta) = i\left(\frac{\pi}{3}\right) + \frac{V_i(2 - d)}{3\omega L}\left(\theta - \frac{\pi}{3}\right) \quad (25)$$

for $\phi + \pi/3 \le \theta \le 2\pi/3$

$$i(\theta) = i\left(\phi + \frac{\pi}{3}\right) + \frac{V_i(2 - 2d)}{3\sigma L}\left(\theta - \phi - \frac{\pi}{3}\right) \quad (26)$$

for $2\pi/3 \le \theta \le 2\pi/3 + \phi$

$$i(\theta) = i\left(\frac{2\pi}{3}\right) + \frac{V_i(1 - 2d)}{3\omega L}\left(\theta - \frac{2\pi}{3}\right) \quad (27)$$

for $\phi + 2\pi/3 \le \theta \le \pi$

$$i(\theta) = i\left(\phi + \frac{2\pi}{3}\right) + \frac{V_i(1 - d)}{3\omega L}\left(\theta - \frac{2\pi}{3} - \phi\right). \quad (28)$$

Equating $i(0) = -i(\pi)$ and solving, we obtain

$$i(0) = \frac{V_i}{3\omega L}\left[\frac{2\pi d}{3} - d\phi - \frac{2\pi}{3}\right]. \quad (29)$$

Using $i(\theta)$, the supply-side dc-link current can be reconstructed using the input bridge switching function and is shown in Fig. 4(b). From this, the average output power is calculated to be

$$P_0 = \frac{V_i^2}{\omega L}d\phi\left[\frac{2}{3} - \frac{\phi}{2\pi}\right]. \quad (30)$$

The above results apply for $0 \le \phi \le \pi/3$.

For $\pi/3 \le \phi \le 2\pi/3$, a similar set of equations can be derived. The average output power for ϕ in this range can then be found to be

$$P_o = \frac{V_i^2}{\omega L}d\left[\phi - \frac{\phi^2}{\pi} - \frac{\pi}{18}\right]. \quad (31)$$

Based on $i(\theta)$, the important parameters such as the transformer kVA, input and output capacitor ripple current, and peak device stresses can be found. The transformer kVA, for instance, is

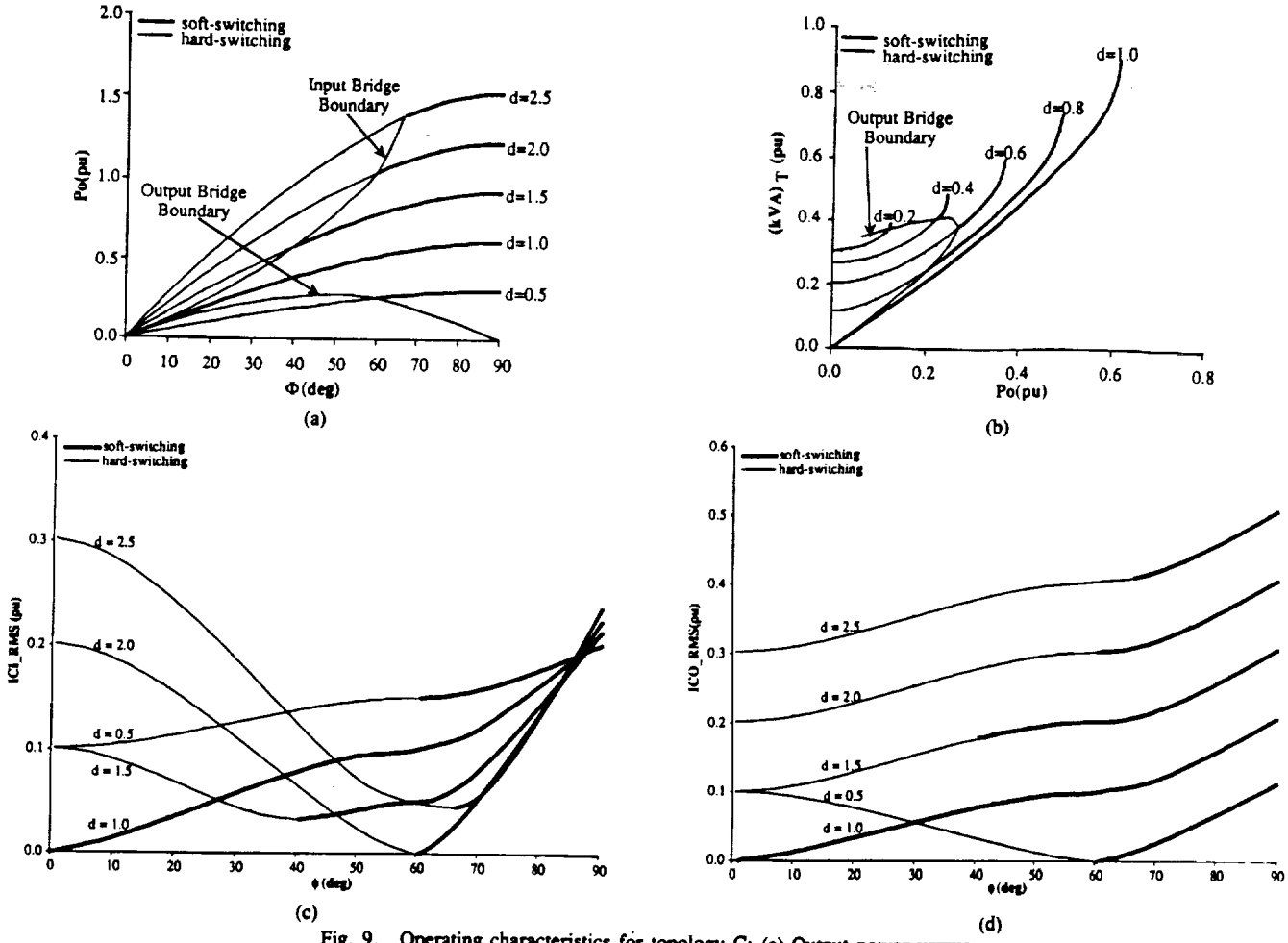


Fig. 9. Operating characteristics for topology C: (a) Output power versus ϕ, with d as parameter; (b) transformer kVA versus output power, with d as parameter; (c) input filter capacitor r.m.s. current versus ϕ, with d as parameter; (d) output filter capacitor r.m.s. current versus ϕ, with d as parameter.

calculated as in (9) and can be reduced to

$$(\text{kVA})_T = \frac{V_i(1+d)\,I_{\text{rms}}}{\sqrt{2}}.$$

Fig. 9(a) is similar to Fig. 7(a) and shows the variation of P_0 as a function of ϕ for different values of d. Once again, the curve for $d = 1$ shows wide range of control, i.e., from zero power for $\phi = 0$ to maximum power for $\phi = \pi/2$. The output bridge boundary corresponds to the soft-switching locus for a diode output bridge. This locus is derived by finding the value of $\phi = \phi_c$ such that $i(\phi_c) = 0$. For $0 \le \phi \le \pi/3$ this yields the lower boundary d_l:

$$d_l = 1 - \frac{3\phi}{2\pi}. \tag{32a}$$

The upper boundary governs the transition for the input bridge between natural commutation and soft switching. This corresponds to the relationship $i(0) = 0$, which yields d_u:

$$d_u = \frac{1}{1 - \dfrac{3\phi}{2\pi}}. \tag{32b}$$

For $\pi/3 \le \phi \le 2\pi/3$, the lower and upper boundaries are obtained to be

$$d_l = \frac{3}{2} - \frac{3\phi}{\pi} \tag{33a}$$

$$d_u = \frac{1}{\dfrac{3}{2} - \dfrac{3\phi}{\pi}}. \tag{33b}$$

Fig. 9(b) shows the kVA rating of the transformer for $0 \le d \le 1$ as a function of the output power. The locus corresponding to output diode bridge operation is also plotted. Once again, it can be seen that for the maximum power transfer point (0.267 pu) on the output bridge boundary (pertaining to the output bridge operating as a diode bridge) the minimum transformer kVA required is 0.391 pu, which gives a transformer utilization of 68%. Now, for the same transformer kVA, the output power can be increased to 0.351 pu at $d = 1$ by virtue of an active output bridge. The transformer utilization has thus been increased by 31%.

Fig. 9(c) and 9(d) shows the ripple current in the input and output capacitor filters as a function of d and ϕ. It will be seen that for $d = 0.5$ and $\phi = 60°$, the output current ripple goes to zero. At the maximum power transfer point $P_0 = 0.46$ pu, $\phi = 50.1°$ and the output current ripple is 0.095 pu while the input current ripple is 0.0925 pu. For lower values of d, the

output current ripple increases. However, under all conditions, the ripple is substantially smaller than for either of the single-phase converters. Clearly, given the operating range of the converter, an optimization is possible that yields the smallest total filter size.

The analysis of the two dual-bridge converter topologies has yielded interesting and fairly counterintuitive results in terms of overall system power density. It is not clear whether the resulting system, using transformer leakage inductances,gives higher power density than a conventional hard-switched dc/dc converter in which the leakage elements are parasitics. In order to examine these issues better, a fundamental component model of the system is invoked and analyzed next.

Fundamental Model Analysis

Conceptually, each of these circuits can be viewed as an inductor (the transformer leakage inductance) driven at either end by a controlled square-wave voltage source. The voltage sources are phase shifted from each other by a controlled angle ϕ. To simplify the analysis, the square-wave voltage sources are replaced by their fundamental components. Fig. 10 shows the fundamental model. Note that this model can also be treated as a per phase model for Topology C. The model is identified to the familiar synchronous-machine equivalent circuit and may be expected to demonstrate similar properties. The inductance L is analogous to the series inductance of the machine. The input (V_{fi}) and output (V'_{fo}) voltage sources can be viewed as the internal EMF and terminal voltage, respectively. The angle ϕ is commonly referred to as the torque angle. Since all circuit quantities are sinusoidal at a single frequency (the switching frequency), a phasor analysis can be carried out. The steady-state current phasor I through the inductor is given as

$$I = \frac{V_{fi} - V'_{fo}}{X_L} \tag{34}$$

where

$$V_{fi} = V_{fi}\langle 0\rangle$$
$$V'_{fo} = V'_{fo}\langle -\phi\rangle$$
$$X_L = j\omega L$$

and where ω = switching frequency. Note that for a square-wave input voltage of peak amplitude V_i, the rms fundamental component V_{fi} is given as

$$V_{fi} = \frac{2\sqrt{2}\,V_i}{\pi}.$$

Similarly, for the output,

$$V_{fo} = \frac{2\sqrt{2}\,V_o}{\pi}.$$

Hence, the output power is given as

$$P_o = \mathrm{Re}[V'_{fo}I^*] = \frac{V_{fi}V'_{fo}}{\omega L}\sin(\phi) = \frac{V_{fi}^2}{\omega L}d\sin(\phi) \tag{35}$$

where

$$d = \frac{V'_{fo}}{V_{fi}}.$$

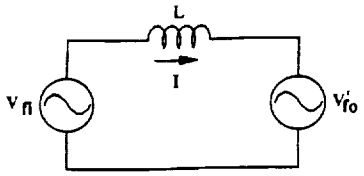


Fig. 10. Fundamental model of the dual bridge dc/dc converter.

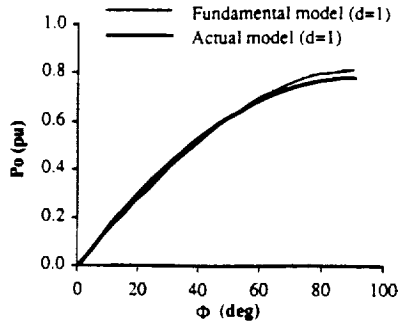


Fig. 11. Comparison of the output power versus ϕ, at $d = 1$, from the fundamental model and actual model.

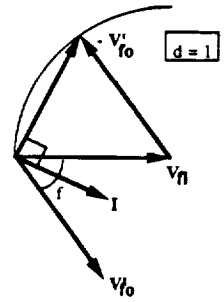


Fig. 12. Phasor diagram for the fundamental model illustrating the relative positions of the current and voltage phasors for soft switching at $d = 1$.

Equation (35) is identical to that for a synchronous machine. Fig. 11 shows a plot of the fundamental output power (normalized to the power base defined in (11) for $d = 1$. The actual output power for Topology B for $d = 1$ is also shown on the same figure. The good correlation justifies the validity of the fundamental model.

To appreciate the relationship between ϕ and d for soft-switching conditions, phasor diagrams based on the fundamental model can be very helpful. Again, as a reminder the soft-switching constraints dictate that the inductor current I lags the input voltage V_{fi} and leads the output voltage V_{fo}'. For instance, Fig. 12 shows the phasor diagram for $d = 1$. As ϕ is varied over the range $0-\pi/2$, the current phasor, I always remains between the phasors V_{fi} and V_{fo}', thus satisfying the preceding soft-switching constraints for this entire range of ϕ. This conforms to our actual model.

Considering the issue of transformer size may also be easier in the fundamental model. First, let us evaluate the transformer kVA based on the fundamental model (for Topology B) from (9):

$$(\mathrm{kVA})_T = \frac{V_{fi}^2(1+d)}{2\omega L}\sqrt{d^2 - 2d\cos(\phi) + 1}. \tag{36}$$

Assume that for a given $(\mathrm{kVA})_T$, transformer size is inversely proportional to the frequency, given the core material. Given the task of designing a transformer for a conventional hard-switched dc/dc converter, one chooses $d = 1$ and L small for maximiz-

ing transformer utilization. This implies a small value for $\phi = \phi_h$. If this transformer is designed for frequency $\omega = \omega_h$, then from (35) and (36), one can derive

$$\omega_h L = X_L = \frac{V_{fi}^2}{P_o} \sin(\phi_h) \tag{37}$$

$$(\text{kVA})_{T(h)} = P_o \sec\left(\frac{\phi_h}{2}\right). \tag{38}$$

This is approximately equal to P_0 since ϕ_h is assumed small. Thus the transformer size for hard switching will be proportional to S_h, where

$$S_h = \frac{(\text{kVA})_{T(h)}}{\omega_h} = \frac{P_o}{\omega_h} \sec\left(\frac{\phi_h}{2}\right). \tag{39}$$

Similarly, examining the soft-switched converter, we can see that maximum power transfer occurs at $\phi = \phi_s = \pi/2$ and $d = 1$. Under these conditions and at a frequency ω_s, we find for the same ratings

$$\omega_s L = \frac{V_{fi}^2}{P_o} \tag{40}$$

$$(\text{kVA})_T = \sqrt{2}\, P_0 \tag{41}$$

$$S_s = \frac{(\text{kVA})_{T(s)}}{\omega_s} = \frac{\sqrt{2}\, P_o}{\omega_s}. \tag{42}$$

Comparing the sizes of the two transformers, we can see that

$$\frac{S_s}{S_h} = \frac{\sqrt{2} \sin(\phi_h)}{\sec\left(\frac{\phi_h}{2}\right)} \tag{43}$$

Since typical values for ϕ_h are in the 2°–10° range, it can be seen that significant reduction in transformer size is possible by switching to a scheme where the leakage inductances are the current transfer elements. This comparison is further strengthened when the losses resulting from interaction of diode reverse recovery and leakage inductance are considered for a current-source-output dc/dc converter.

Comparison of Proposed Converters

The three converters proposed have been presented in detail including sufficient information for the development of operating characteristics. In order to better compare the three topologies, Table I presents the detailed specifications for various components based on the equations and curves presented in the paper. The design is denormalized so as to conform to a specification of 50 kW with an input voltage of 200 Vdc, an output voltage of 2000 Vdc, and a switching frequency of 50 kHz. Optimum design points for each of the topologies are shown in the table

Examining peak device stresses, the three-phase dual bridge offers the lowest ($V_{ce} I_c$) stress at (1.17 *load kW) as opposed to a factor of 3.45 for Topology A. However, Topology B shows a slightly higher stress at 1.19 pu. Moreover, in Topology C the peak-device turn-off current is lower than the peak current in the transformer. Similar conclusions are seen from the transformer kVA ratings. Topology A exhibits poorest transformer utilization and very high current stresses. The total input and output filter requirements are seen to be lowest for Topology C, as

TABLE I
Summary of Component Stresses
(P_o = 50 kW; V_i = 200 Vdc; V_o = 2000 Vdc; f = 50 kHz)

	Topology A	Topology B	Topology C
d	0.58	1	1
β(°)	180	—	—
ϕ(°)	—	28.78	35.41
Device Specs.			
Input Bridge			
No. of Active Devices	4	4	6
Peak voltage (V)	200	200	200
Peak current (A)	861.48	297.57	293.46
$V_{pk} * I_{pk} / P_o$	3.45	1.19	1.17
Output Bridge			
No. of Active Devices	4 (diodes)	4	6
Peak voltage (V)	2000	2000	2000
Peak current (A)	50.68	29.76	29.35
$V_{pk} * I_{pk} / P_o$	2.03	1.19	1.17
Transformer Specs.			
I:N	1:17	1:10	1:10(Y-Y)
Peak pri. volts (V)	200	200	133/ph
Peak pri. amps (A)	861.48	297.57	293.46
RMS pri. amps (A)	497.52	281.4	197.29/ph
Peak sec. volts (V)	2000	2000	1333/ph
Peak sec. amps (A)	50.68	29.76	29.35
RMS sec. amps (A)	29.27	28.14	19.73/ph
kVA	78.64	56.28	55.7
P_o/kVA	0.64	0.89	0.89
L (μH)	0.77	1.1	0.89/ph
Filter Specs.			
Input			
Cap. volts (Vdc)	200	200	200
Cap. RMS amps (A)	429.75	129.15	48.43
kVA	85.95	25.83	9.69
Output			
Cap. volts (Vdc)	2000	2000	2000
Cap. RMS amps (A)	14.63	12.92	4.84
kVA	29.26	25.83	9.69
Operation	1-Quadrant	2-Quadrant	2-Quadrant

expected, because of the higher ripple frequency. Overall, Topology C seems to be the most viable option for the application. However, the biggest disadvantage is the practical realization of a three-phase symmetrical transformer with identical leakage inductances in each phase [12]. Moreover, it requires two additional devices on each bridge as opposed to Topology B.

A value of L has been specified in order to attain the desired specifications. The actual choice of ω and L will depend on the core material and detailed transformer design. It is anticipated that limitations on transformer size minimization will be imposed by the weak scaling factors that govern how the leakage inductances reduce with size as operating frequency is increased. Although it has been shown that the dual-bridge converters are inherently capable of higher power density, Topology A has many desirable characteristics. For higher output voltages, where active devices may be unable to operate, diode rectifiers may be the only alternative along with topology A. Further, for applications where the reliability or cost penalties of additional gate turn-off devices is unacceptable, again Topology A may be the only viable option.

Experimental Results

An experimental proof-of-concept unit based on the proposed Topology B was fabricated in the laboratory using bipolar junction transistor as the switching device. The unit was rated for 1 kW for a switching frequency of 20 kHz. Fig. 13 shows the primary and secondary voltage and the primary current

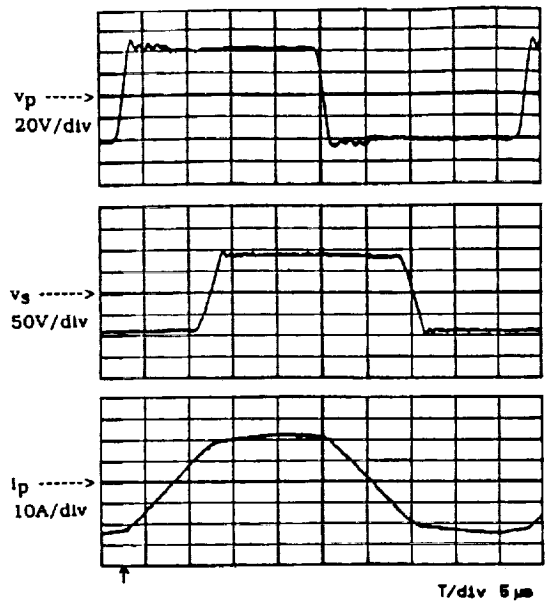


Fig. 13. Oscillograms of transformer voltages and currents from the 1-kW proof-of-concept unit of topology B.

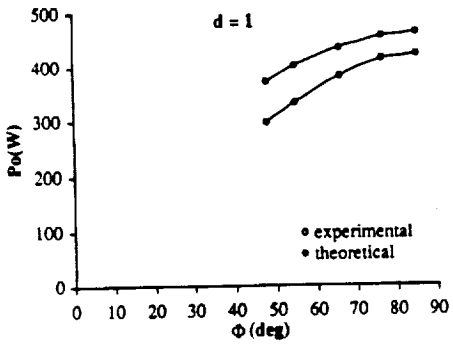


Fig. 14. Comparison of the experimental and theoretical output power versus ϕ characteristic at $d = 1$ for topology B.

waveforms for $d = 1$. The waveforms demonstrate the soft-switching capabilities for all the devices on both the bridges. Fig. 14 shows the variation in the output power with phase shift. The trend in the experimental curve is seen to closely match that of the theoretical. Output power increases as phase shift increases.

Conclusion

Three new dc/dc converter topologies suitable for high-power-density high-power applications have been presented in this paper. All three circuits operate in a soft-switched manner, making possible a reduction of device switching losses and an increase in switching frequency. Along with soft switching, all proposed circuits utilize the leakage reactance of the ac-link transformers as active current transfer elements and eliminate problems of interaction between these leakage inductances and diode reverse recovery. The dual-bridge topologies are also capable of buck-boost operation and bidirectional power flow, although that aspect has not been analyzed in detail in this paper.

The current transfer mode of operation makes it easier to parallel multiple modules for extending the power capacity of the system. The use of a three-phase ac-link system dramatically reduces the capacitor ripple currents, making it possible to use high-power-density multilayer ceramic capacitors. The dual-bridge converters are also seen to offer an unexpected gain in the power density attainable as a result of the controlled action of the two bridges. Since the snubbers used are purely capacitive, these would supplement the internal device capacitance, giving a clean power structure. The total number of system components is also seen to be minimal—the input and output filter capacitors, two bridges, and one transformer. All device and component parasitics are seen to be used favorably.

The dual-bridge topologies proposed have the most favorable characteristics including:

- small number of components
- low device and component stresses
- zero (or low) switching losses for all devices
- small filter components
- high efficiency (no trapped energy)
- bidirectional power flow
- buck-boost operation possible
- low sensitivity to system parasitics
- parallel operation possible as a result of current transfer.

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DESIGN CONSIDERATIONS FOR HIGH POWER DENSITY DC/DC CONVERTERS

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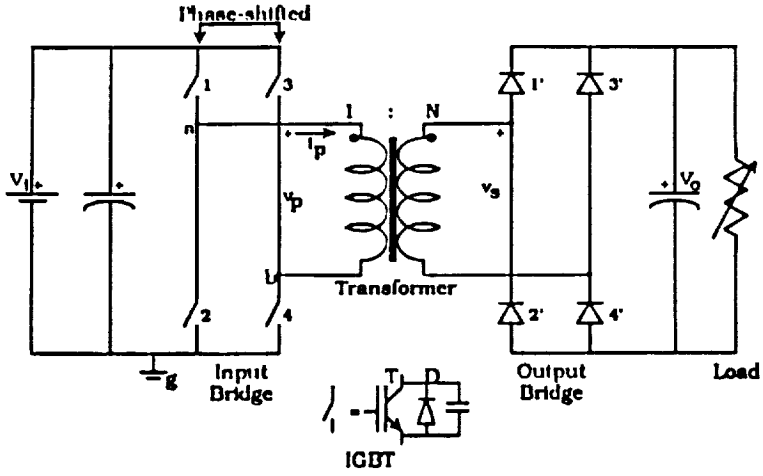
INTRODUCTION

This paper investigates the requirements for high power density dc/dc converters for high power applications. The dual bridge dc/dc converter, proposed in [1], was seen to be a viable concept in terms of reduced stresses and component requirements, and was also seen to be suitable for high power operation. Further work on the new topologies is presented here with particular emphasis in generating first pass numbers for the power densities and efficiencies actually attainable.

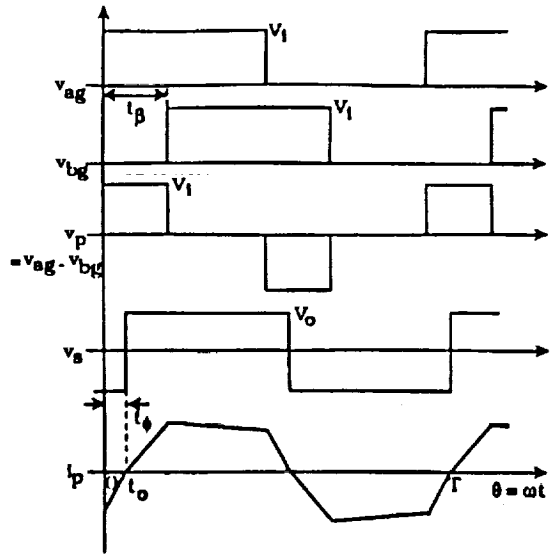
First, a brief review of the proposed topologies with experimental waveforms obtained from a 1.5 kW proof-of-concept unit built to demonstrate the principle of soft-switching in the proposed converter is given. Subsequent sections investigate trade-offs and fundamental design issues involved in the reduction of the major loss components in the circuit, in particular, the converter and transformer losses. Finally, a split-up of the projected weights of the various components in the two proposed topologies is presented for a dc/dc converter rated at 50 kW and operating at a frequency of approximately 50 kHz. The converter is to be designed for a 200V dc input and a 2000V dc output.

PROPOSED TOPOLOGIES

The two proposed topologies, the phase shifted single active bridge converter (Topology A) and the dual-active bridge converter (Topology B), have been treated exhaustively in Reference [1]. Figures 1a and 1b show the two circuits with their operating waveforms. Both the topologies are "minimal" in structure in that they consist of the input and output filters, the two device bridges and a transformer, all components essential for a dc/dc conversion process. The proposed topologies operate at a constant switching frequency and exhibit soft switching for reduced switching losses. Moreover, both the circuits utilize the leakage inductance of the transformer as the main energy transfer element thus rendering the filters on both the input and output sides purely capacitive. However, with a passive diode bridge, as in topology A, the leakage impedance limits maximum power transfer. The maximum power transfer point for topology A occurs at d = 0.58 [1]. With the active output bridge, as in topology B, reactive excitation for the secondary winding can be supplied from the output side, thus allowing a dramatic increase in the power that can be transferred through the same transformer at a given frequency. Table 1 compares the stresses and kVA ratings of the various components for the two proposed topologies A and B operating under identical specifications. Also, shown in Table 1, for purpose of comparison, are the stresses and kVA ratings for the Series Resonant DC/DC Converter [2], regarded as the state-of-the-art in high power, high power density dc/dc converter technology, operating under the same voltage and power specifications. However, the operating frequency for this converter was selected as 10 kHz, since the devices used were

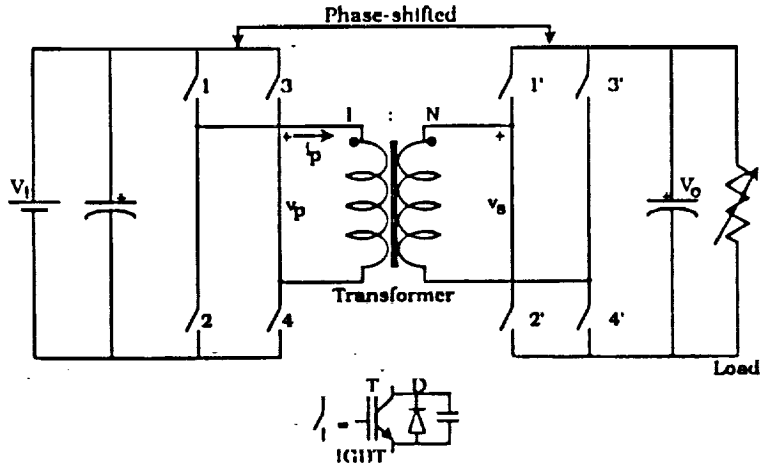


Schematic of Phase-Shifted Single Active Bridge DC/DC Converter(Topology A)

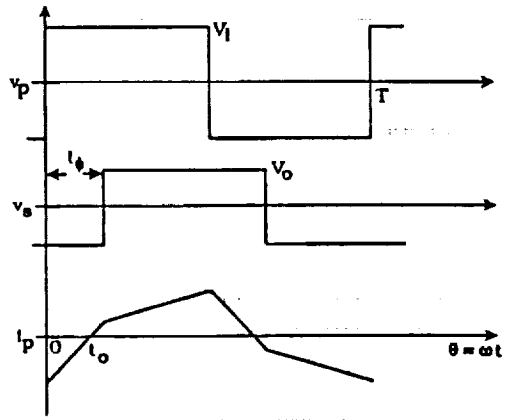


Operating Waveforms for Topology A

Figure 1a



Schematic of Single-Phase Dual Active Bridges DC/DC Converter(Topology B)



Operating Waveforms for Topology B

Figure 1b

thyristors. Topology B exhibits lowest device stresses and component kVA ratings. The 1.19 pu stress on the switch elements compares very favourably against the theoretical value of 1 pu for a hard switched pwm converter. The transformer and the total filter capacitor ratings, for topology B, are also significantly lower. It is clear that the proposed topology B constitutes a better converter choice for this application.

The high voltage output requirement seems to make the use of active output bridges difficult, as devices rated in the kilovolt range are limited in terms of switching speed. The high power density needed mandates a high switching frequency. Thus, a modular approach is necessary for realizing high powers. Given the high voltage specification, a series connection of active bridges is proposed as an effective approach. The resulting topology is shown in Figure 2. However, for purposes of computation, a single active output bridge is considered.

An experimental model for the rated specifications, mentioned earlier, is currently under fabrication. However, a proof-of-concept unit has been built with a rating of approximately 1.5 kW and Figure 3 shows waveforms demonstrating the principle of soft switching in this converter. As seen from the "soft" voltage transitions, all devices operate essentially under zero voltage switching. This, as will be explained in the following section, results in the low turn-off switching losses. Figure 4 shows the experimentally obtained steady state power transfer characteristics as a function of the phase shift. As seen this compares favourably with the theoretically obtained results.

TABLE 1
(Pout = 50kW, Vin = 200Vdc, Vout = 2000Vdc)

	Topology A (f = 50 kHz)	Topology B (f = 50 kHz)	SRC (f = 10 kHz)
1. Device Specs.			
a. No. of active devices	4+(4 diodes)	8	4+4(diodes)
b. Ipk (primary)(A)	861.5	297.6	555.6
c. (Vpk * Ipk)/Pout	3.45	1.19	2.22
2.Transformer Specs.			
a. Transformer-kVA	78.6(d=0.58)	56.3(d=1)	76.3(d=0.71)
b. Leakage Inductance(μH) (Primary referred)	0.77	1.1	9.2
3. Reactive Elements			
a. Input filter Capacitor-kVA	85.9	25.8	54.5
b. Output fiter Capacitor-kVA	29.3	25.8	22.0
c. Resonant Capacitor-kVA	-	-	138.9

Of importance in assessing the power density are the losses incurred in the system. The transformer and semiconductor losses are the dominant loss factors, and these are analyzed next in detail.

CONVERTER LOSSES

Converter losses are a strong function of switching frequency and switching methodology. For high power density converters, necessarily operating at high frequencies, the use of zero-voltage/zero-current switching techniques, to minimise the switching losses, is an attractive alternative. In the proposed topologies (A and B), all devices operate under conditions of zero-voltage switching. The turn-on of any device is initiated while its anti-parallel diode is conducting. This ensures that the device naturally takes over as the diode current reverses, and

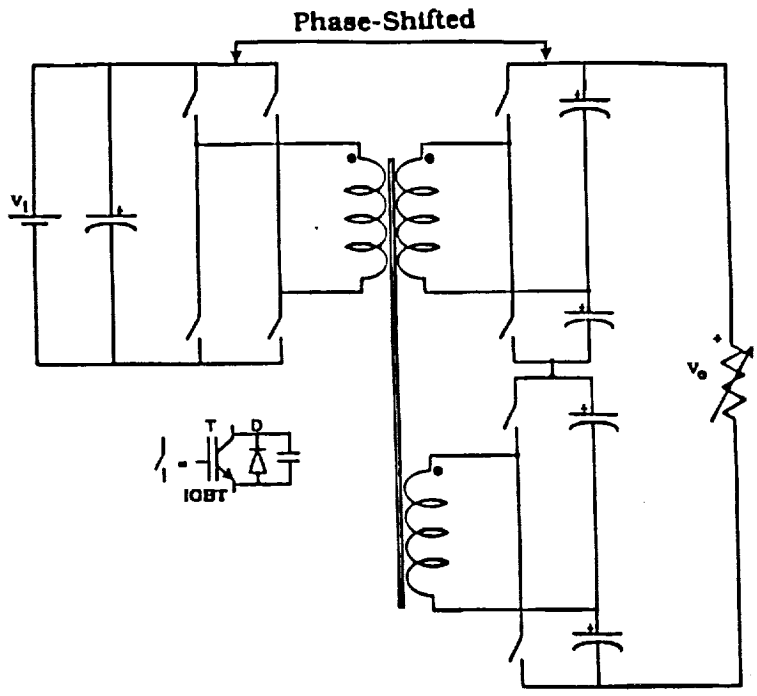


Figure 2 Schematic of Series Connected Single-Phase Dual Active Bridge DC/DC Converter for High Voltage Outputs

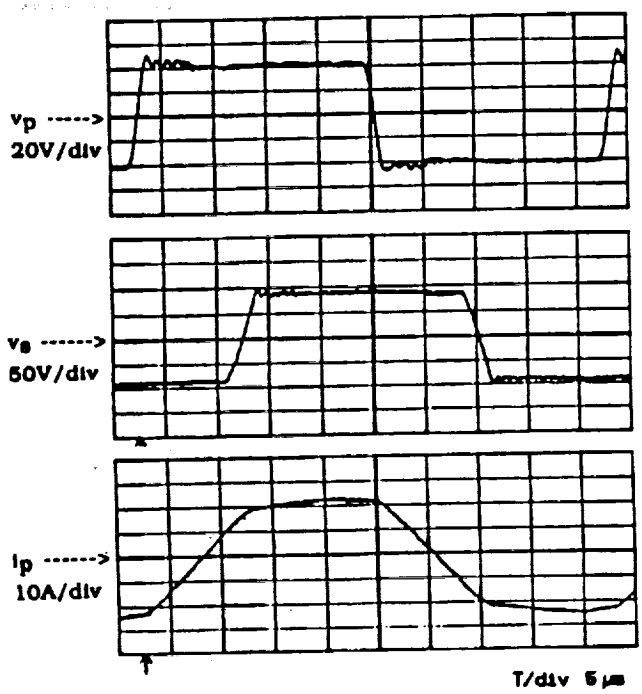


Figure 3 Oscillograms of transformer voltages and current from 1.5 kW proof-of-concept unit, demonstrating soft-switching capability of proposed topology

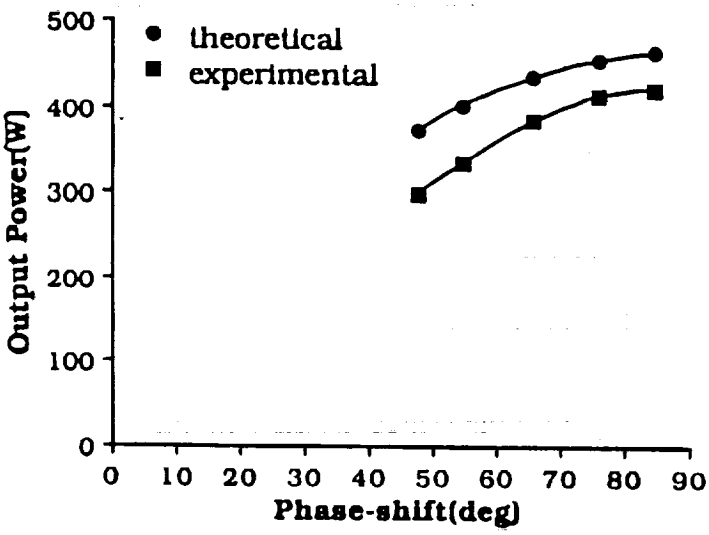


Figure 4 Output Power vs Phase-shift from proof-of-concept unit for d = 1 (Topology B)

more importantly under almost zero-voltage conditions. This also prevents the circuit from being subjected to the high voltage stresses which are typical of inductive circuits in the presence of diode reverse recovery effects. Zero-voltage turn-off is implemented by purely capacitive snubbers. The turn-off process must always be initiated when the device is carrying a certain minimum current. The rate of rise of voltage across the device during its turn-off is governed by the snubber capacitor. Typically, such circuits are oversnubbed to ensure near zero-voltage turn-off.

An extensive analysis was carried out to ascertain the switching and conduction losses for each of the proposed topologies. The device of choice at this time, is the Insulated Gate Bipolar Transistor (IGBT). Although the MOS Controlled Thyristor (MCT) seems to be a better alternative, availability of adequately rated devices is not anticipated in the near future. A typical model for the turn-off switching waveform is shown in Figure 5 [3]. As the dominant component of the switching loss occurs during turn-off, an expression is derived for this loss and is shown in Equation 1.

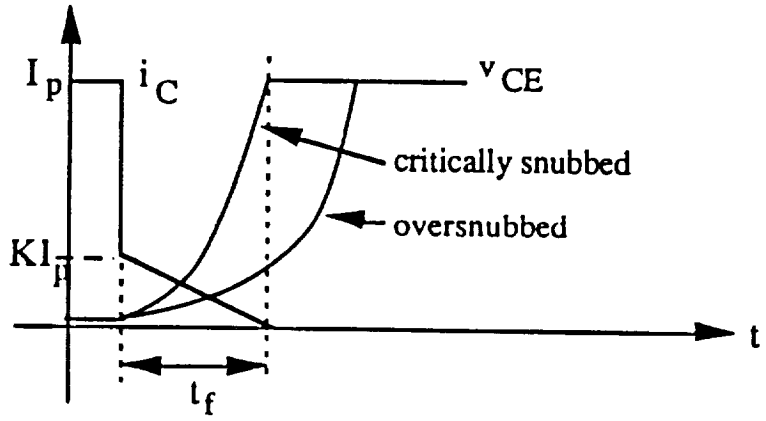


Figure 5 Model of IGBT turn-off switching waveform

$$P_{sw} / \text{device} = \frac{f I_p^2 t_f^2 (4 - 3K)K}{48C} \qquad \ldots(1)$$

where, f is the switching frequency, C is the snubber capacitance, and I_p, t_f and K are as shown in Figure 4. Equation 1 is valid as long as C is greater than the critical value.

The conduction losses are based on the asumption that the currents flowing through the transistor or its anti-parallel diode are linear. This is a fair assumption for high frequency transformers, since the dominant parameter is the leakage inductance. The average current through each transistor and diode are first derived and multiplied by their respective on-state voltages to give the conduction loss. For instance, the expressions for the transistor and diode conduction losses, for Topology B, are as shown in Equations 2 and 3.

$$P_{con} / \text{transistor} = 0.5\, f\, V_T \left[\frac{1}{f} - t_o - t_\phi\right] |I_p| \qquad \ldots(2)$$

$$P_{con} / \text{diode} = 0.5\, f\, V_D\, [t_o - t_f]\, |I_p| \qquad \ldots(3)$$

where, V_T, V_D are on-state voltages of the transistor and diode respectively, t_ϕ is the phase-shift between input and output bridges, and t_o is the instant of time where the current reverses direction in the positive half cycle(see Figure 1b).

Table 2 summarises these loss figures for both the topologies at a rated output power of 50kW while switching at 50 kHz. The device fall time, t_f, which is essentially the tail time was selected as 0.5 μs and K as 0.25, from the manufacturer's data sheet [4]. V_T and V_D were selected as 3V and 1V respectively. The switching loss figures can be lowered even further by selecting larger snubber capacitors. The high conduction losses evident for all the topologies is a consequence of the device type. IGBTs have substantially higher on-state voltages than MOS-Controlled Thyristors (MCTs). With on-state voltages of 1.3V, assumed for the MCT [5], a 50% reduction in the conduction losses is realized for both the topologies. The switching losses for the MCTs have been computed assuming a turn-off switching behaviour which is similar to the IGBT.

TABLE 2
(Comparison of Projected Semiconductor Losses)
Pout = 50 kW, Vin = 200 Vdc, Vout = 2000Vdc, f = 50 kHz

	Topology A		Topology B	
	IGBT	MCT	IGBT	MCT
Switching Losses(W)	668.8	668.8	257.6	257.6
Conduction Losses(W)	2273.9	1116.7	1684.7	801.2
Total(W)	2942.7	1785.5	1942.3	1058.8

Comparing the losses in topologies A and B, the higher current stress in circuit A gives higher conduction and switching losses. The snubber capacitors are the smallest possible for ensuring that the device currents reach zero prior to an application of full voltage across the device.

TRANSFORMER LOSSES

The transformer is by far the dominant component, in terms of weight, for the proposed topologies. High power density requirements of 0.2-0.25 kg/kW with voltage outputs in the order of kilovolts, calls for a rigorous design methodology. The issues of core material selection and winding geometries for the minimum core and copper losses at the highest possible switching frequency, are addressed in this paper. Again, the upper limit on the switching frequency is governed to a large extent by the device type and allowable switching losses.

The characteristics of a good core material include high operating frequency, low specific core loss and low power/weight ratio. In the light of these properties, two candidates, Ferrites and Permalloy 80 are considered. Both the proposed circuit topologies use the transformer leakage inductance as the energy-transfer element. The power transferred through the transformer is given by Equations 4 and 5 for both topologies.

$$\text{Pout(topology A)} = \frac{dV_{in}^2(4ft_\beta - d^2 - 4f^2t_\beta^2)}{8fL} \qquad \ldots(4)$$

$$\text{Pout(topology B)} = \frac{dV_{in}^2 t_{\phi}(1 - 2ft_{\phi})}{L} \qquad \ldots(5)$$

where, V_{in} is the input dc voltage, d is the ratio of the output dc voltage reflected to the primary side to the input dc voltage, f is the switching frequency, L is the leakage inductance, and t_{β}, t_{ϕ} are as shown in Figure 1. For the ratings specified, the required leakage inductance can be calculated and is shown in Table 1. It can be seen that the leakage inductances are small enough to require the use of some low leakage transformer design techniques.

Consequently, the shell-type of core (constructed from E-E cores) is preferred, as it can realize low leakage inductances. Table 3 shows the weight and core losses associated with the above two core materials at their typical operating flux densities and frequencies. The calculations are based on the TDK Ferrite(H7C4) (EI70) and 0.5 mil Magnetics Permalloy 80 (ME1565), for a typical current density of 750 c.mil/A. The selected ferrite core is the largest standard (in terms of size) available. Hence, a stack of 3 such cores is needed to achieve an equivalent power handling capability as that of the selected Permalloy 80 core. The resultant ferrite transformer, having a larger proportion of the copper covered by the window, has a lower leakage inductance. However, it does have higher core losses and weight. On the other hand, the ferrite material does lend itself as the better choice for switching frequencies above 50 kHz in the vicinity of 100 kHz or more. Of course, the choice of the final frequency rests upon the switching device. With IGBTs, as is presently planned, it seems that 50 kHz or higher should be easily possible. As is evident from Table 3, the ferrite core is heavier. But, one must also account for the amount of copper required for each of the cores and then compare the overall power densities. It can be shown that for the selected core sizes and a window fill factor of 0.5, the weight of copper required for the Permalloy 80 core is almost four times that for the ferrite. This results in an overall power density for the ferrite transformer of 0.09 kg/kW as opposed to 0.14 kg/kW for the Permalloy 80 transformer. In the light of these trade-offs, and given the lower cost of ferrite cores, they are considered a more viable option for core material.

TABLE 3
(Transformer Comparison)

	Ferrite(H7C4)	**Permalloy80(0.5mil)**
Power (kW)	45	49
Frequency (kHz)	50	20
Bmax (T)	0.2	0.5
Iron Losses (W)	103	83
Core Weight (kg)	2.48	1.87
Copper Weight (kg)	1.33	5.19
Transformer Weight (kg)	3.81	7.06
Power Density (kg/kW)	0.09	0.14

The second issue of the optimum winding arrangement for the lowest copper losses is a fairly involved task. Copper loss is extremely sensitive to the leakage flux distribution in the window region, and is thus dependent on the core and winding geometries. To investigate this problem, extensive use was made of a high frequency transformer design program [6]. This program takes as inputs, pertinent core, window and winding section dimensions. It incorporates the conductor type as well as relevant data for each winding. The Fourier components of the current flowing in each winding, must also be specified. It then computes the copper losses for each winding section after accounting for the skin and proximity effects. The skin effect losses can be controlled by choosing conductor dimensions in the order of a skin

depth. The proximity effect, which is a manifestation of the leakage field in the window region, needs careful consideration.

To study this effect, a ferrite shell-type core, as mentioned earlier, was selected. The primary winding is foil-wound, since it allows a good fill factor at high currents, while the high voltage secondary is wound with Litz wire. The primary winding consists of two sections connected in parallel. Two arrangements, namely concentric and split windings are studied, as shown in Figure 6a. Figure 6b depicts the leakage flux distribution in the window region, obtained from magnetostatic finite element analysis, for each arrangement. Table 4 shows the split-up of the copper losses. It is evident that the concentric arrangement is more efficient than the split one. The startling difference in the copper losses in the two configurations can be explained by considering that - (i) the leakage field is much stronger in the split arrangement, which results in higher proximity effect losses, which are directly proportional to the square of the H-field; and (ii) the mutual orientation of the flux-lines and the winding sections (in the split arrangement, flux-lines are almost orthogonal to the Foil plane, thus presenting a large area for eddy current paths).

TABLE 4
(Comparison of Copper Losses in the two Winding Arrangements)
Pout=50kW, f=50kHz

	Concentric	**Split**
Primary(W)	144	301
Secondary(W)	32	297
Total(W)	176	598

Since, the leakage inductance of the transformer is used as the main energy transfer element in the proposed topologies, it needs to be carefully controlled and uniformly distributed. This design objective is a relatively difficult task to meet in the conventional transformers discussed above. Coaxially wound transformers, discussed in detail in reference [7], offer a viable solution for realizing low and controlled leakage inductance, with the added benefits of reduced forces in the transformer, lower core saturation and robust construction.

A 50 kW, 50 kHz transformer using coaxial winding techniques has been fabricated. The core material was selected as Ferrite(H7C4) with the core-volume, core-geometry, current density and copper fill factor maintained the same as that for the transformer arrangements discussed above. The following are the measured quantities:

Transformer Test Data

Magnetizing inductance(primary referred) = 250 μH

Leakage inductance(primary referred) = 0.15 μH

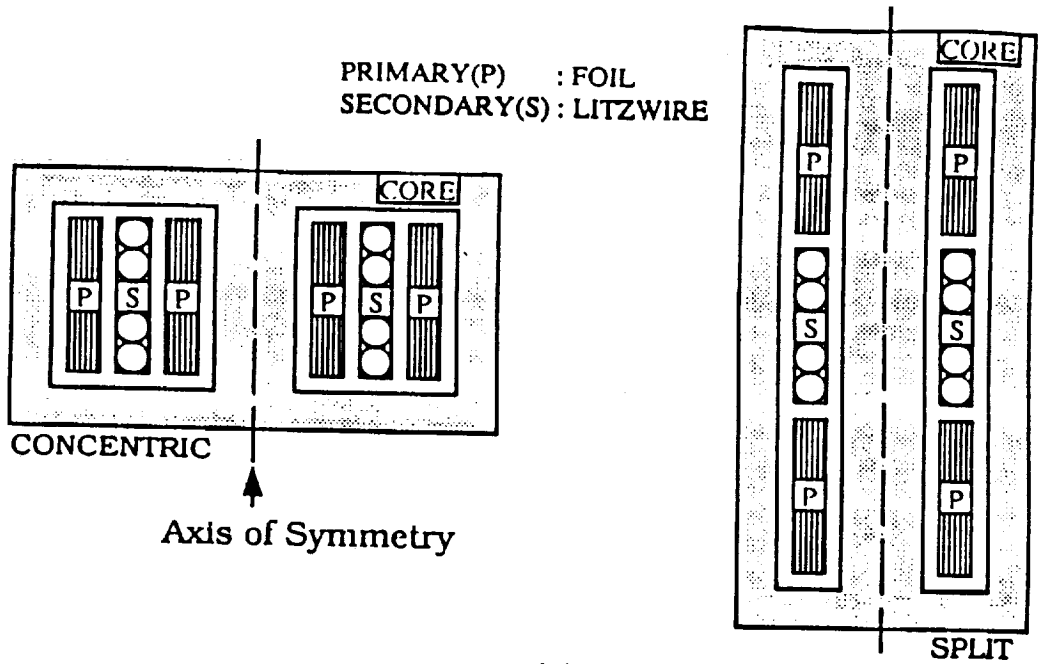
Core Loss = 70 W at 0.15T, 50 kHz, 200V(primary, square wave)

Copper loss = 180 W at 230 Arms(primary), 50 kHz

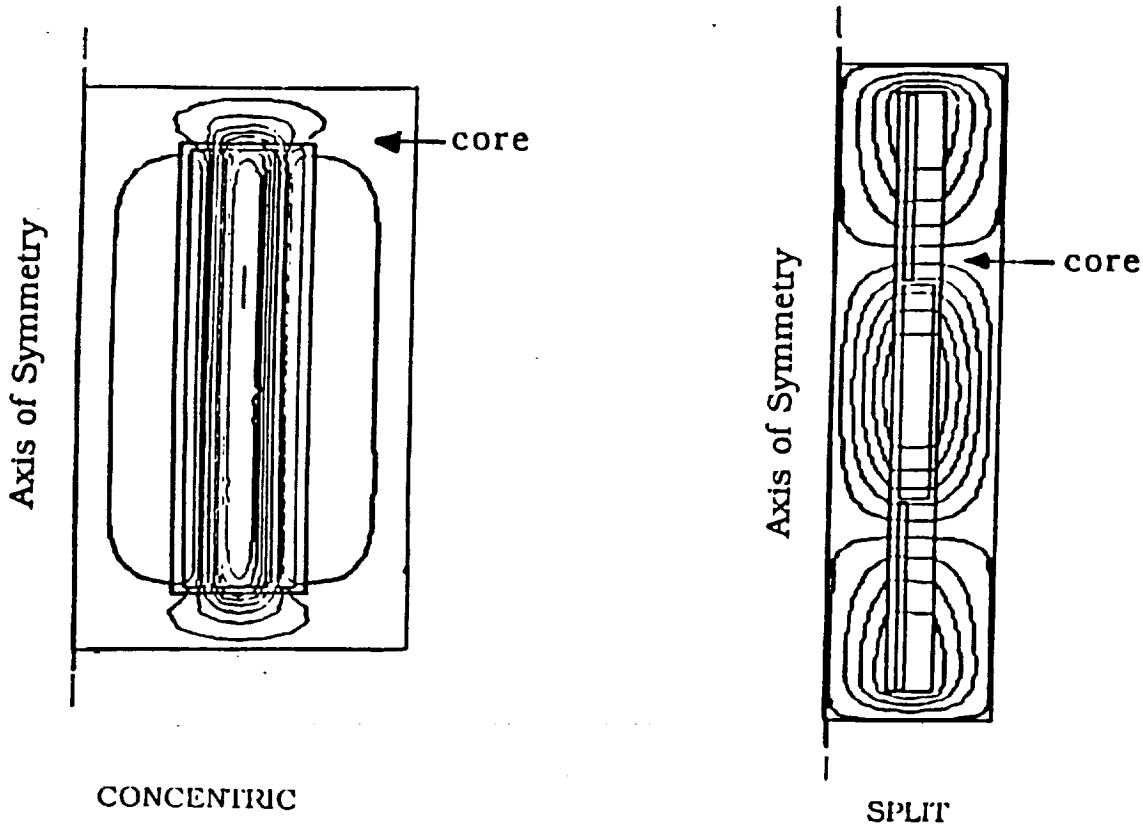
Transformer weight = 3.83 kg

Projected kVA = 46 kVA

Projected Efficiency = 99.4 %



(a)



(b)

Figure 6 (a)Schematic of the two winding arrangements for Shell-type Transformer
(b)Leakage field distribution in the window region for each arrangement

Projected power density = 0.083 kg/kW

Figure 7 shows the secondary voltage and primary current measured under short-circuit test conditions, with the input bridge devices switching under soft-switching conditions.

PROJECTED WEIGHT AND EFFICIENCY

Table 5 gives a rough projection of the weights for the various components in the proposed topologies, operating at the rated specifications. The filter capacitors selected, are state-of-the art Multi-Layer Ceramic capacitors (MLCs), which offer the highest ripple current rating for a given volume and weight. The total weight of these capacitors, required for topology B, is seen to be only 0.8kg, of which 0.45kg is for the input filter. On the other hand, the weight for conventional commutation grade capacitors, which would be the next best choice in terms of ripple current rating, is estimated at 2.7kg, for the input side. The weights for the filter capacitors do not include the mounting ground and supply plates, which are included with other hardware. The overall power density of 0.2 kg/kW, for topology B, is in the desired vicinity of the target of 0.2 - 0.25 kg/kW. It would be appropriate to mention here that the series resonant converter [2], using thyristors as devices, commutation grade capacitors for the filters and Permalloy 80-core transformer has an overall power density of 0.9 kg/kW, for the same power rating. Table 5 also shows the projected efficiencies for the two topologies with IGBTs (and MCTs) as the switching devices and the ferrite core (with the concentric winding arrangement) transformer. The improvement in efficiency with using MCTs is a direct consequence of the lower device conduction losses.

TABLE 5
(Weight and Efficiency Comparison)
Pout=50kW, f=50kHz

	Topology A (kg)	Topology B (kg)
Transformer(ferrite core)	5.9	4.2
Filter Capacitors(MLC)	1.6	0.8
Device+Hardware	3.0	3.0
Gate Drivers	0.5	1.0
Mounting Hardware	1.6	0.8
Total	12.6	9.8
Power Density	0.25 kg/kW	0.20 kg/kW
Efficiency	93.9% (96%)	95.7% (97.4%)

(The efficiency figures in parentheses are for MCTs)

Top Trace: Secondary voltage, 50 V/div
Bottom Trace: Primary Current, 100 A/div

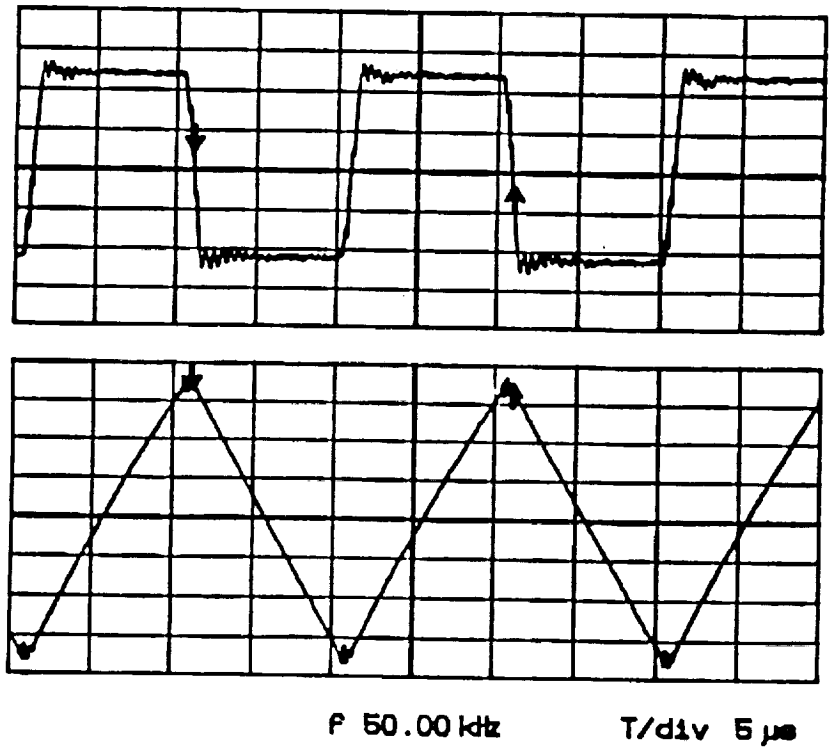


Figure 7 Oscillograms under short-circuit test conditions, for the 50 kW, 50 kHz coaxially wound transformer

CONCLUSIONS

Further work on the two proposed dc/dc converter topologies, the phase-shifted single active bridge converter (Topology A) and the dual-active bridge converter (Topology B), has been presented. Major emphasis is laid upon the fundamental issues and trade-offs involved in the minimization of the dominant loss factors occuring in the semiconductor devices and the transformer. It is seen that Topology B is the favoured option in terms of reduced device stresses and lower filter and transformer kVA ratings. For a 50 kW converter, switching at 50 kHz with IGBTs as devices, the total device losses incurred in Topology B is 34% lower than Topology A. As shown, the conduction loss is the major component and can be reduced by almost 50% by using MCTs as devices. Unfortunately, these devices, in the required high ratings, are still unavailable. Extensive analysis, has demonstrated that the Ferrite-core shell-type transformer offers a power density of 0.09 kg/kW as opposed to 0.14 kg/kW for the Permalloy 80-core. In addition, the concentric winding arrangement for the transformer turns out to be more efficient than the split arrangement. A 50 kW, 50 kHz coaxially wound transformer has been fabricated to primarily demonstrate its suitability for low and controlled leakage inductance. Finally, a comparison of the weight split-up for the two topologies is done. A projected overall power density of 0.20 kg/kW along with an efficiency of about 95%, for Topology B, makes it a more attractive alternative. A 50 kW unit, switching at 50 kHz, with input and output dc voltages of 200V and 2000V respectively is currently under fabrication and results will be reported in a future paper.

Acknowledgements

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DESIGN CONSIDERATIONS FOR HIGH POWER HIGH FREQUENCY TRANSFORMERS

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Abstract

This paper addresses design considerations for transformers utilized in high-power high-frequency dc/dc converters. Major areas of concern are core-material selection, minimization of copper losses due to skin and proximity effects, and the realization of controlled leakage inductances. Core-loss characteristics for various high frequency materials are presented, and the influence of various winding arrangements on the copper losses is also demonstrated. This paper also examines co-axial winding techniques (used commonly in high frequency transformers), as a reasonable solution for containing the leakage flux within the interwinding space, and hence preventing it from permeating the core giving lower core losses and avoided localized heating. Added benefits of this technique are reduced forces within the transformer, lower copper losses and robust construction. The performance of an experimental 50 kW, 50 kHz unit is reported in the paper.

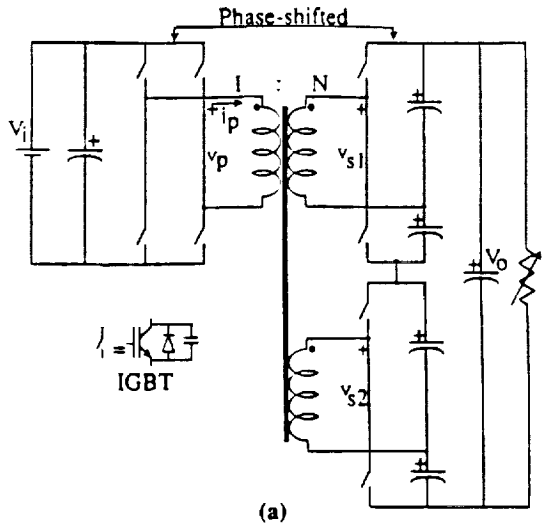
Introduction

A considerable effort has been directed towards high-frequency transformers in the very low power range [1,2,3,4]. This paper investigates some of the requirements for transformers used in high-power (multi-kilowatt), high-frequency dc/dc converters, in particular the dual active bridge (DAB) converter proposed in [5]. The topology is attractive because of zero voltage switching, low component stresses, smaller transformer size and low sensitivity to system parasitics. The transformer leakage inductance is used as the main energy transfer element, and essentially supports the entire voltage across it.

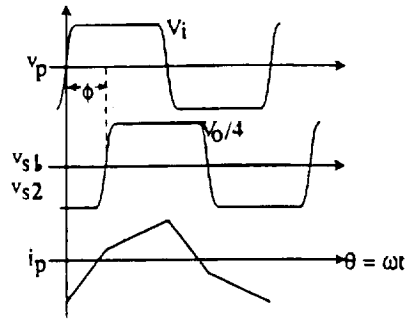
The DAB converter circuit is shown in Figure 1a. The converter topology is seen to be minimal in nature, as it incorporates input and output filter capacitors, two device bridges and the isolation transformer, all components necessary for any dc/dc conversion process. The input and output bridges are switched so as to generate a resonant transition square wave at each transformer terminal, with the output half-bridges switching in synchronism. The two square waves are phase shifted from each other by an angle ϕ, and the resulting voltage is applied across the transformer leakage inductance. The relevant operating voltage and current waveforms are shown in Figure 1b. The power transferred from primary to secondary can be calculated to be,

$$P_o = \frac{V_i^2}{2\pi f L} d\phi\left[1 - \frac{\phi}{\pi}\right] \qquad \ldots(1)$$

where, V_i is the input dc voltage, d is the ratio of the output dc voltage reflected to the primary side to the input dc voltage, f is



(a)



(b)

Fig. 1 (a)Schematic of 1 ph Dual Active Bridge DC/DC Con--verter, with cascaded Output Bridges for high volt--age outputs
(b)Relevant operating waveforms

the switching frequency, L is the leakage inductance and ϕ is the phase-shift between the two bridges. The optimum design point is seen to correspond to a dc conversion ratio (referred to the primary side) of unity (d = 1). For the ratings specified, (V_i=200 Vdc, V_o=2000 Vdc, f=50 kHz and P=50 kW) the leakage inductance necessary is seen to be 1.06 μH. This demands the use of low leakage transformer design techniques. Further, as the entire voltage is supported by the leakage reactance, it is important that the leakage field be distributed as uniformly as possible to avoid localized heating of the core.

Broadly speaking, the two fundamental issues in the design of any high-power high-frequency transformer are minimum losses and low leakage inductance. The two loss

components associated with the transformer, namely core and copper losses, are strongly related to the frequency. Core loss, for a given frequency and flux density, is material dependent. Consequently, as a first step in the design process, an investigation of various high frequency core materials is essential. Copper loss in the transformer is extremely sensitive to the leakage flux distribution in the window region, which in turn is dependent on the core and winding geometry. The influence of different conventional winding arrangements on the winding losses and leakage inductance, will be studied.

As mentioned earlier, in the proposed dc/dc converter, the presence of a certain amount of leakage inductance (governed by the rated power, frequency and design point) is crucial to the operation of the converter, since it functions as the main energy transfer element from one dc voltage source to the other. On the other hand, too high a value restricts maximum power transfer. In essence, the leakage inductance needs to be carefully controlled. This design objective is a relatively difficult task to meet in conventional transformers. Coaxial windings, used primarily for very high frequency (radio frequency range) transformers, seem to offer an interesting and viable option. The latter part of this paper addresses such winding techniques.

Selection of Core Material

The characteristics of a good core material include low specific core losses (defined as losses per unit volume or per unit mass) at high operating frequencies, high saturation flux density, high power/weight ratio, and good thermal and mechanical properties. In the light of these characteristics, three candidates, Ferrite PC40 Permalloy80(0.5mil) and Metglas2605SC(1mil) were investigated. Table 1 lists some of their salient properties.

To characterize these core materials, the specific core losses were measured for different frequencies over a wide range of flux densities under square wave voltage excitation. These tests were carried out owing to the unavailability of such data for square wave excitation. A half-bridge inverter, using Power MOSFETs as switches, was fabricated to generate the square wave voltage across a 4-turn foil-wound coil mounted on the core under test. The core loss was measured by integrating the product of the voltage and current on the coil on the LeCroy 9400 digital oscilloscope. The core loss figure includes the winding losses, which were estimated to be small enough (within 1%) to be neglected without much error. Figures 2a & 2b show specific core losses (measured as mW/cc) plotted as a function of the flux density on a log-log scale for the three candidate materials at 25 kHz and 50 kHz respectively.

It is seen that Metglas exhibits the highest core losses for both the test frequencies over the entire range of test flux densities, and is hence not considered to be a viable core material for our application, given the high power density and high efficiency constraints. The Permalloy80 (0.5 mil) material appears to be the most promising of the three materials for all the test frequencies. On the other hand, even though the Ferrite material has higher losses than the Permalloy80, the former offers a wide range of core geometries. In particular, for high power, low leakage transformer designs, the shell-type of transformer built from E-E cores is the most desirable. Such core shapes are readily available in the Ferrite material. Moreover, there is a distinct cost advantage in going for Ferrite cores.

It is now important to look at the copper losses. The following sections involve a study of two possible winding arrangements, conventional and coaxial. Various interleaving arrangements of winding sections would fall under the category of conventional windings.

TABLE 1
(Test Core Material Properties)

	Ferrite(PC40)	Permalloy80	Metglas2605SC
Type	Ceramic	Tape-wound	Tape-wound (Amorphous)
Composition	Fe_2O_3 50% MnO 50%	Ni 80% Fe 16% Mo 4%	Fe 81% B 13.5% Si 3.5% C 2%
Bm(T)	0.2	0.5	0.75
μ	2300	30000	50000
Ω-m	6.5	0.57	1.25
Shape	E,I,U, Toroids, Pot, etc.	Toroids, Cut C-cores	Toroids, Cut C-cores

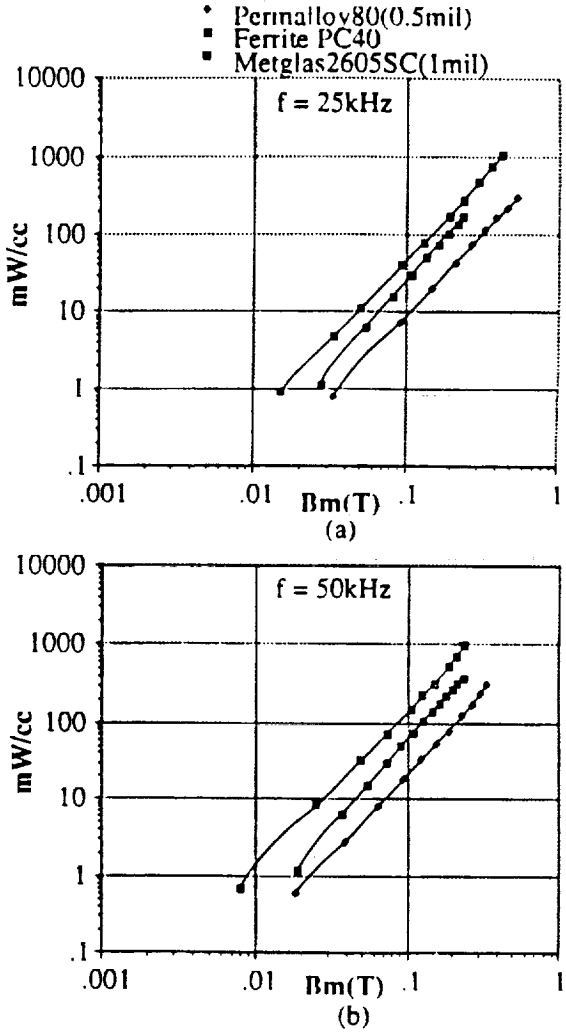


Fig. 2 Specific Core losses for the three candidate magnetic materials: (a) at 25 kHz; (b) at 50 kHz

Conventional Winding Arrangements

The primary objective of this section is to study the influence of the various conventional winding geometries on the copper losses. Copper losses in a high frequency transformer are predominantly due to skin and proximity effects, which are collectively called eddy current effects.

Skin effect associated with a conductor carrying alternating current, is the redistribution of the current towards the surface due to the magnetic field generated by this current. The resultant increase in the current density can be seen, from a circuit viewpoint, as an increase in the effective resistance of the conductor. Consequently, for a given current the I^2R losses would increase. This phenomenon is strongly related to the frequency. Proximity effect is the phenomenon in which circulating eddy currents are induced in the conductor by time-varying magnetic fields generated from nearby current carrying conductors. These eddy currents generate extra losses and are also strongly related to the frequency and magnitude of the external field.

The two losses can be expressed as,

$$P_{skin} = F * I^2 \qquad ...(2)$$

$$P_{prox} = G * H^2 \qquad ...(3)$$

where, F is the effective resistance due to skin effect of the conductor, G is the proximity effect factor, I is the current in the conductor, and, H is the external magnetic field caused by surrounding currents. F and G are functions of frequency, conductor type (foil, litz wire, or solid round wire), dimensions and material.

Minimization of winding losses, due to the eddy current effects, in high frequency transformers is a fairly challenging task and involves, firstly, the selection of the proper conductor type and dimensions and secondly, an understanding of the influence of the winding geometry on the leakage (or, stray) field distribution in the window region. It is important to calculate this leakage field to assess the proximity effect winding losses.

To appreciate the influence of the conductor type on the effective resistance due to skin effect, for instance, three standard conductor types, viz. foil, litz wire and solid round wire were considered. For each conductor type the cross-sectional area was kept constant, to keep the dc resistance/unit length, R_{dc}, fixed. The effective resistance due to skin effect for each conductor type was calculated as given in [6,7,8]. A standard litz wire was selected, consisting of 329 strands and a total cross-sectional area of 16585 cmils (1 cmil = $\pi/4$ mil^2, where, 1 mil = 25.4 μm). Keeping this as the common cross-sectional area, and choosing f = 50 kHz, the effective resistance for each conductor type, was computed. The thickness of the foil was selected as 2δ, where δ (skin depth) ~ 12 mils at f = 50kHz (for copper). Table 2 summarizes the effective resistance for each conductor type based on the above considerations. As expected the solid round conductor shows the highest increase in effective resistance, and is certainly not suitable as a conductor type for high frequency applications. Foil and litz wire show very little change in their effective resistances from the dc value. Of course, as foil thickness is increased its effective resistance goes up. The choice between the two conductor types, for high frequency transformer applications, is thus dependent on various design trade-offs including relative window dimensions, window fill factor, number of turns, etc.

As a first consideration, the choice of core geometry is dictated by the low leakage inductance desired, and also, the winding arrangement. The use of shell-type core for conventional transformers, made from E-E cores, is seen to be desirable. This, in turn, leaves us with Ferrite as the core material of choice (for reasons mentioned in the last section).Other attractive geometries such as pot-cores, are not available for the high power levels of interest.

TABLE 2
(Effective Resistance due to Skin Effect for the three conductor types, f = 50kHz, δ ~ 12 mils)

	R_{dc} (mΩ/m)	F (mΩ/m)	% Change
Foil (thickness = 2δ)	2.0229	2.2571	11.6
Solid Round	2.0229	6.1756	205.3
Litz (329 strands)	2.0229	2.0233	0.02

To address the issue of the influence of winding geometry on leakage flux distribution, three typical conventional winding arrangements, labelled X, Y and Z, shown in Figure 3

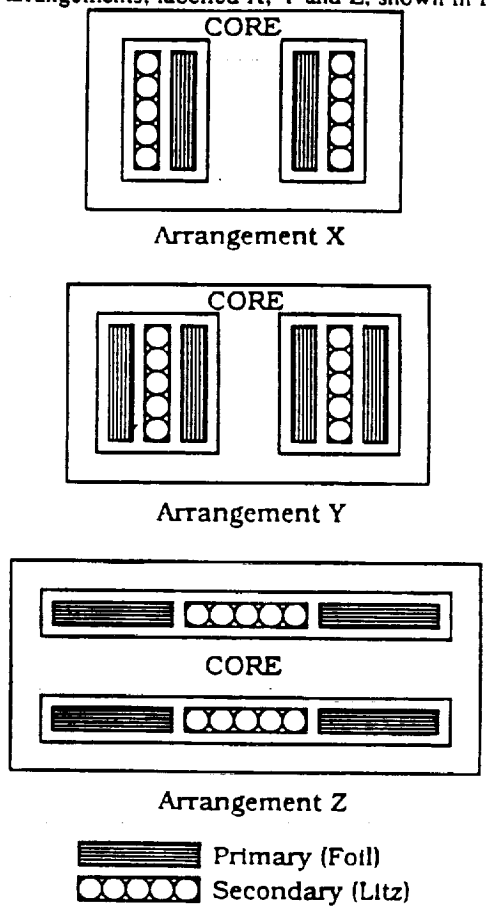


Fig. 3 Three conventional transformer winding arrangements

were studied. Arrangement X consists of one primary and one secondary winding wound concentrically on the centerpost of a shell-core. Arrangement Y consists of one secondary winding sandwiched between two primary windings, which are connected in parallel. All the winding sections are wound concentric to the centerpost. Arrangement Z consists of the same winding sections as in Y, with the sections now stacked vertically, concentric to the centerpost. The two primary sections are connected in parallel. To analyze the copper losses, the transformer, for each winding arrangement, was designed for the actual specifications, viz, 50kW, 50kHz, 200V primary and two secondary windings rated at 1000 V each, maintaining the same amount of copper in the window area. Due to the unavailability of a finite element eddy current solver package, the computation of these losses was done with the aid of a high frequency transformer design program [7].

This software referred to as "TID" by its author takes as inputs pertinent core, window and winding section dimensions. It also accounts for the conductor type (foil, litz wire or round) with all its relevant dimensions. The Fourier components of the current flowing in each winding must also be specified. It then computes the total winding losses by calculating the skin effect and proximity effect losses separately for each frequency component and simply adding all the terms together. The loss due to skin effect is computed as given in Equation (2). As seen from the proximity effect Equation (3), the field distribution in the window region must first be calculated. This is done using the method of images, which in essence consists of replacing the effects of a boundary on an applied field by simple distributions of currents behind the boundary line, the desired field being given by the sum of the applied and the image fields [9].

Setting the maximum operating flux density at 0.2T, typical for the selected Ferrite material, the required core cross-sectional area can be calculated from the transformer voltage relation, given below,

$$V_{pri} = 4N_{pri} B_m f A_c \qquad ...(4)$$

where, N_{pri} is the number of primary turns, f is the frequency of operation and A_c is the core cross-sectional area. Note, since the excitation voltage is square-wave, the form factor is set to 4. At this point, however, the number of primary turns is also not known. Considering the high levels of primary current and the high turns ratio required, N_{pri} was set to 3. Moreover, to maintain a reasonably high fill factor, and given the constraint of providing sufficient insulation at the high voltage levels, a foil-type of primary conductor was selected. The core cross-sectional area can now be determined from Equation (3), and further the core centerpost dimensions can be fixed.

The primary foil thickness was set to approximately 2δ, where δ is the skin-depth (at 50kHz). The conductor type for the secondary windings, consisting of 15 turns each, was selected as litz wire. To determine the amount of copper area, the current density and operating rms current at full power must be known. The current density was selected as 500 cmil/A. For the rated current levels in each winding and the specified current density, the primary foil dimensions could be completely defined. For the secondary litz wire, an equivalent AWG of 6 was needed. Next, as required by the "TID" program the winding and window dimensions, and the first three Fourier series components of the primary and secondary current at the design point were specified.

Table 3 summarizes the copper losses, computed by the program, for each of the three arrangements - X, Y, Z. It is seen that the arrangement Y is the best, in terms of incurring least copper losses. The reduction in copper losses in going from arrangement X to Y can be explained as follows. A split up of the primary winding into two sections in Y, results in a peak field intensity half of that of X, in the window region. The ampere-turn waveform in the window region for the two winding arrangements is shown in Figure 4 to give an idea of the relative peak field intensities. Since, the proximity effect losses are proportional to the square of the leakage field, arrangement Y experiences lower proximity effect losses as compared to that of X. Recalling that the primary windings are

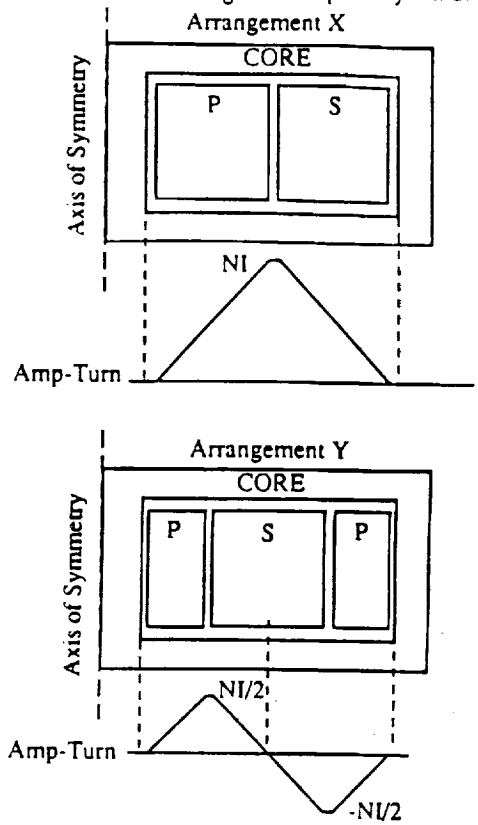


Fig. 4 Idealized Amp-turn waveform in the window region for the two winding arrangements

foil-wound, in arrangement Z it is seen that the flux lines, as shown in Figure 5 enter the primary foil-plane perpendicularly. Eddy currents are readily induced in the foil-plane, as expected, since a large surface area is available for conduction. These eddy currents, as a result of the pronounced proximity effect, give rise to the very large copper losses observed in Table 3. The higher secondary losses in arrangement Z are due to the fact that the narrower window gives rise to much stronger leakage fields.

TABLE 3
(Copper losses in the 3 winding arrangements)
(P_O = 50kW, V_i = 200Vdc, V_O=2000Vdc, f = 50kHz)

	X	Y	Z
Primary(W)	179	144	301
Secondary(W)	97	32	297
Total(W)	276	176	598

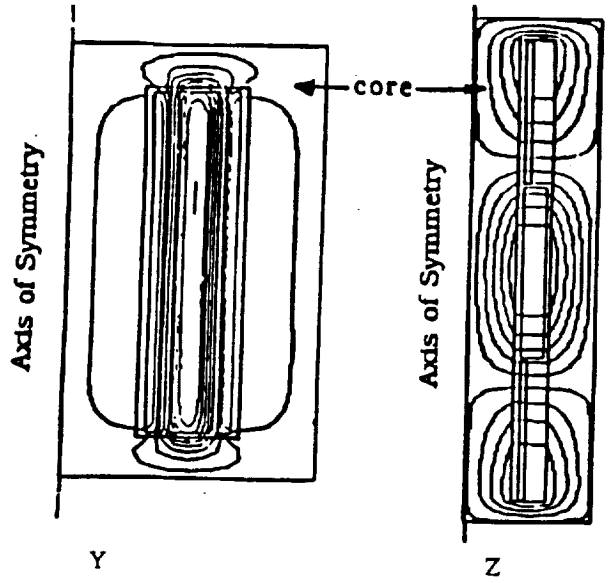


Fig. 5 Leakage flux plots under loaded conditions for
(a)Winding arrangement Y
(b)Winding arrangement Z

In short, to minimize copper losses, windings must be sectionalized and interleaved to reduce field intensities in the window region. Moreover, these sections must also be arranged such that the flux lines are directed parallel to foil planes.

As seen from the flux plots for the conventional windings, a considerable amount of leakage flux gets coupled into the core. In designs where the leakage flux is small, it may not be very important. However, for converters where the leakage inductance is the main power transfer element, this could contribute substantially to localized saturation of the core, resulting in local hot spots and additional core losses. A preferred technique is the use of coaxially wound transformers, a well-known technology in the area of radio frequency magnetic component design [10, 11].

Coaxial Winding Arrangements

Figure 6a shows a coaxially wound transformer using conductors of circular cross-section, the simplest possible geometry for such transformers. The primary consists of a single turn made from a U-shaped tube of circular cross-section. The thickness of the tube must be maintained within a skin depth, which as calculated before is 12 mils at 50 kHz. However, from the standpoint of mechanical rigidity the thickness of the tube needs to be at least 2 to 3 times this value. The inner secondary winding is of litz wire. The preferred core geometry is toroidal. Multiple toroidal cores can be slipped on the primary winding, depending upon the core area desired.

A point worth mentioning here is with regard to the choice of core material. As far as conventionally wound transformers are concerned, it is seen that the optimum choice of core geometry is the shell-type built from E-E cores, for high power applications. This left us with Ferrite as the material of choice, given the unavailability of such shapes in the Permalloy80 tape-wound material for single-phase applications. On the other hand, for coaxial transformers with circular cross-section, a toroid is the optimum core geometry. Also, from a viewpoint of physical implementation, at higher power levels, the number of turns on the outer tubular winding gets limited to one. This would drastically lower the magnetizing inductance if Ferrite is used as the core material, for a given core cross-section. The much higher permeability of Permalloy80 tape-wound cores and their availability in toroidal shapes, does suggest the suitability of this material for coaxial transformers.

A flux plot for the above arrangement, under loaded conditions, is shown in Figure 6b. This was obtained from a magnetostatic finite element analysis. As expected, the leakage flux is uniformly confined to the region inside the outer tube only. This is the flux due to the inner secondary winding. As mentioned earlier, this is certainly very desirable since the core is free from the effects of any localized saturation.

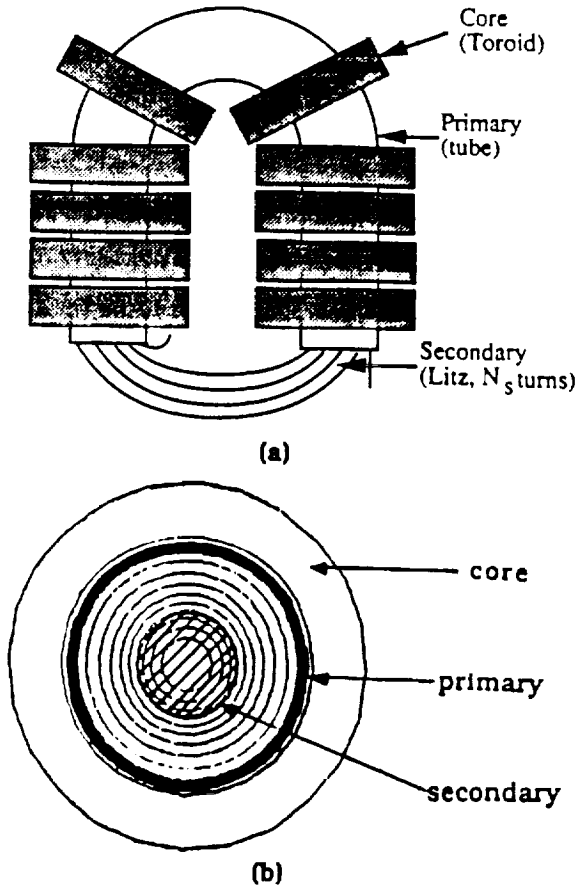


Fig. 6 (a)Layout of 1 ph coaxially wound transformer, with primary tube of circular cross-section
(b)Leakage flux plot from magnetostatic finite element analysis showing all the leakage flux confined within outer primary tube

The leakage flux consists of the internal flux of the secondary winding and the flux within the interwinding space, which is linked by the secondary winding only. Hence, the leakage inductance per unit length can easily be derived as,

$$L_{cir} = \frac{N_s^2 \mu_o}{4\pi}\left[1 + 2\ln\left(\frac{r_{pi}}{r_s}\right)\right] \text{ H/m} \qquad ...(5)$$

where, r_{pi} is the inner radius of the primary tube (outer conductor), and r_s is the radius of the secondary litz wire, and N_s is the number of secondary turns. It is seen from Equation

(5) that for a given N_s as the interwinding space is reduced by decreasing r_{pi}, the leakage inductance decreases. This is the most interesting feature of the coaxial winding, in that the leakage inductance is so easily controllable. In the above derivation, it is assumed that the inner winding is completely enclosed by the outer tubular winding. However, as shown in Figure 5a, this is not true. The portion of the inner winding that is not enclosed, simply contributes to the leakage inductance. If a high leakage inductance is desired, and the interwinding space is at a premium, then the length of the exposed inner winding can be judiciously controlled to achieve the objective.

The transformer is also very robust mechanically. The electromechanical forces on the windings, which could potentially be large enough to damage the transformer core at the high current levels expected, are lower than for conventional designs, as the leakage flux can be controlled and confined within the outer conductor.

Another coaxial winding geometry that has been investigated uses a primary conductor of rectangular cross-section. This facilitates the use of E-E cores, if Ferrites is the core material of choice. Figure 7 shows the cross section of such a coaxial winding, with its leakage flux distribution obtained from the magnetostatic finite element analysis, which assumes uniform current distribution. Under such conditions it appears as if a considerable amount of leakage flux permeates the core, in particular at the corners of the tube, as seen from the flux plot. However, in reality, the leakage fluxes entering or leaving the tube induce eddy currents, which by Lenz's law would tend to oppose this leakage field. The resultant effect, is a redistribution of the current in the outer tube, in such a manner that most of the current is crowded towards the middle portion of each side of the tube. Intuition says that the majority of the resultant leakage field would still stay confined within the outer tube. This proposition remains to be verified, from an eddy current finite element analysis.

Compared to the circular coaxial winding, an equivalent rectangular coaxial would incur higher copper losses because of the eddy currents induced as discussed above. Also, the core could see some leakage flux, in the rectangular coaxial winding, particularly at the corners.

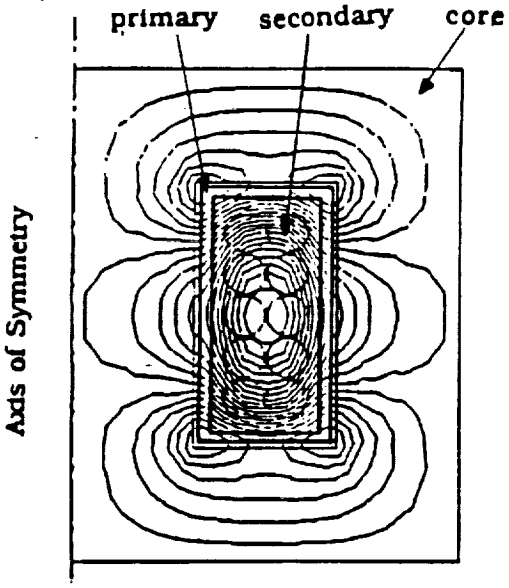


Fig. 7 Leakage flux plot under loaded condition for the 1 ph coaxially wound transformer, with rectangular tube for the primary. Only 1 turn of the primary winding is shown

Two coaxially wound transformers were fabricated for the rated specifications, one with circular tube and the other with rectangular tube for the primary winding. Figures 8a and 8b show the actual layout. The test results are given below:

Test data for Circular Coaxial Transformer:

Core material : Ferrite PC30 (Toroidal cores)
Primary turns = 1
Secondary turns = 5 (two windings)
Magnetizing inductance (primary referred) = 120 μH
Leakage inductance (primary referred) :
Measured = 0.25 μH
Calculated, from eqn. (5) = 0.20 μH (designed for 50 kVA)

Due to limitations in the test set up the core and copper losses could only be measured at half the rated conditions.
Open Circuit Core losses at 0.1 T, 50 kHz = 32.6 W
Short Circuit Copper losses at 120 Arms (primary) = 42.2W

Test data for Rectangular Coaxial Transformer:

Core Material : Ferrite PC40 (E-E cores)
Primary turns = 3
Secondary turns = 15 (two windings)
Magnetizing inductance (primary referred) = 250 μH
Leakage inductance (primary referred) = 0.15 μH
Open Circuit Core losses at 0.15 T, 50 kHz = 70 W (rated)
Short Circuit Copper losses at 230 Arms = 180 W (rated)
Projected kVA = 200 V x 230 Arms = 46 kVA
Transformer weight = 3.83 kg
Projected power density = 0.083 kg/kW
Projected efficiency = 99.4 %

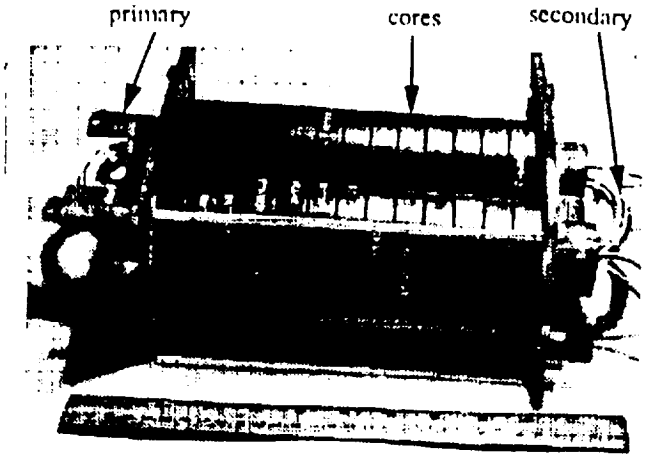
Figure 9 shows the secondary voltage and primary current measured under short circuit test conditions for the coaxial transformer with rectangular tubular primary winding.

The lower magnetizing inductance for the circular geometry is a consequence of lower number of primary turns. The higher leakage inductance for this geometry is to be expected, because of the bigger interwinding space. No comments can be made on the losses in the two geometries, since the circular geometry could only be partially tested. However, the efficiency and power density figures for the rectangular coaxial transformer look very promising.

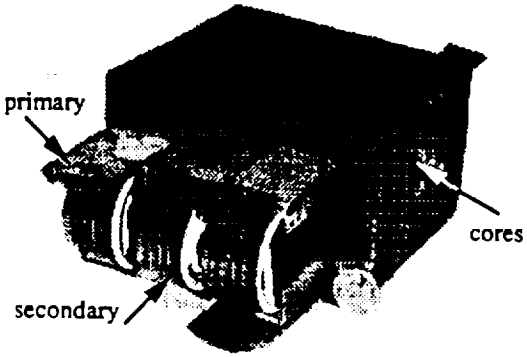
Three-phase Coaxially Wound Transformers

An extension of the 1ϕ dual active bridge dc/dc converter is the 3ϕ version proposed in [5]. The major advantage of the 3ϕ version is the much lower kVA rating of the input and output filter capacitors. This indeed could be an important consideration for high power density converters. However, it is crucial that the leakage inductance, which is the main energy transfer element, be almost identical in each phase of the transformer to ensure balanced operation. This requires that the transformer be physically symmetrical. A possible solution was offered in [5], and is shown in Figure 10. However, the unavailability of suitable core shapes, especially in high frequency materials, would render the construction of such a transformer rather challenging.

Again, coaxial winding techniques offer a viable solution to the construction of such 3ϕ transformers. Figure 11 shows a schematic of a coaxially wound 3ϕ Y-Y transformer. The primary of each phase consists of a straight tube of circular cross section. The star point is realized by shorting the tubes at one



(a)



(b)

Fig. 8 Photographs of fabricated, 50 kVA, 50 kHz, 1 ph coax-
-ially wound transformers
(a) with circular tube primary
(b) with rectangular tube primary

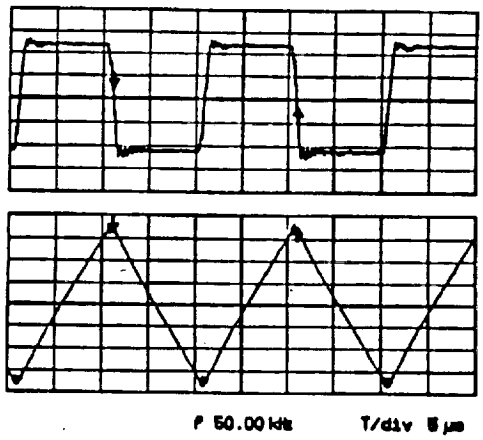
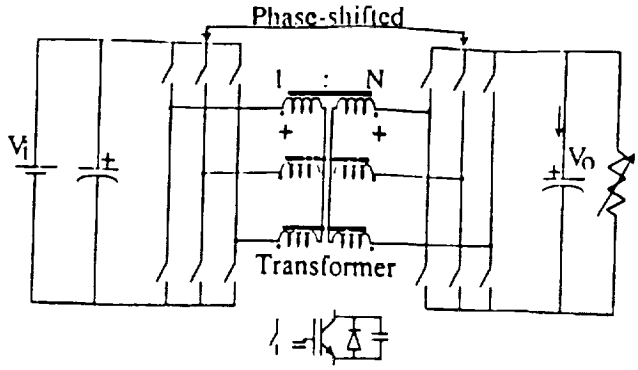
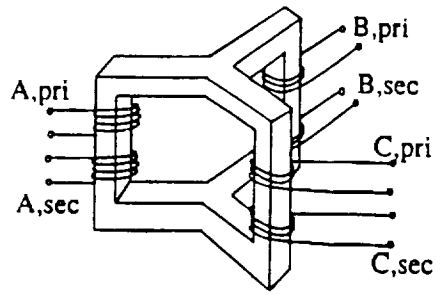


Fig. 9 Oscillograms under short circuit test conditions, for the 50 kVA coaxially wound transformer with rectangular tube primary.
Top trace: Secondary voltage, 50 V/div
Bottom trace: Primary current, 100 A/div



(a)



(b)

Fig. 10 (a) Schematic of 3 ph Dual Active Bridge DC/DC Converter
(b) Schematic of Conventionally wound 3 ph symmet-
-rical transformer

end. Toroidal cores are slipped over each tube to form the magnetic medium. The secondary wire can now be wound inside the primary tube. Only one turn on the secondary is shown. In essence, this construction is nothing but three 1ϕ transformers connected to form the 3ϕ transformer. Although, the structure is completely symmetrical, it suffers from the problem of being unable to drive a single phase load. This can be demonstrated by the following simple analysis. Assume the transformer, is ideal in that it has no leakage inductance and infinite magnetizing inductance. Let the secondary consist of 1 turn (the primary must have 1 turn only). Figure 12 shows the circuit diagram of the 3ϕ Y-Y transformer, with secondary phase 'a' loaded. Applying ampere-turn balance, iA = - ia, iB = -ib, iC = -ic.

Now, $i_b = 0 = i_c$

Hence, $i_B = 0 = i_C$

But, $i_A + i_B + i_C = 0$

Hence, $i_A = 0$

which implies,
$i_a = 0$

This is only possible if the voltage on secondary phase 'a' collapses. Note, the underlying reason for such a behaviour is that no magnetic coupling exists between the phases. To overcome this problem, the secondary can be wound in a "zig-zag" fashion, shown schematically in Figure 13. All the secondary windings have the same number of turns. Repeating the above mode of analysis for single phase loading, we get

$$i_A + i_a - i_b = 0$$
$$i_B + i_b - i_c = 0$$
$$i_C + i_c - i_a = 0$$

But, $i_b = 0 = i_c$

Hence,

$$i_A = -i_a,\ i_B = 0,\ i_C = i_a$$

Thus, it is seen that such a connection allows single phase loading. Figure 14 shows a cross-sectional view of the 3ϕ coaxially wound transformer, with the secondary connected in a "zig-zag" manner.

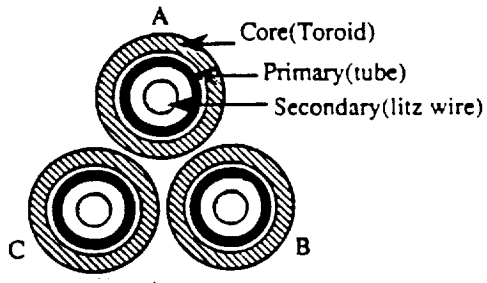


Fig. 11 Layout of a Coaxially wound 3 phase Y-Y transformer

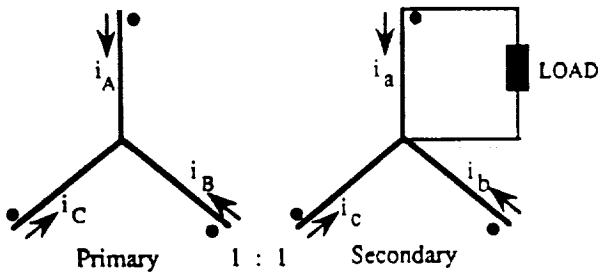


Fig. 12 Circuit Schematic of 3 phase coaxially wound Y-Y transformer, with secondary phase 'a' loaded

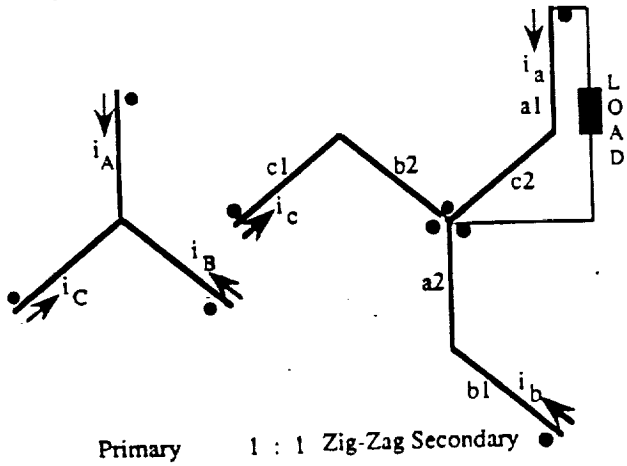


Fig. 13 Circuit Schematic of 3 ph Coaxially wound Y-Y transformer, with secondary connected in a zig-zag manner. Secondary phase 'a' loaded

Thus, it is seen that such a connection allows single phase loading. Figure 14 shows a cross-sectional view of the 3ϕ coaxially wound transformer, with the secondary connected in a "zig-zag" manner.

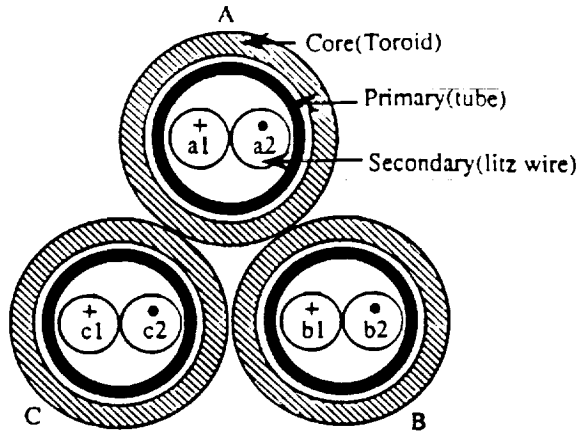


Fig. 14 Layout of 3 ph Coaxially wound Y-Y transformer with secondary connected in a zig-zag manner.

Conclusions

Various design considerations on high power (multi-kilowatt), high frequency transformers have been investigated. Core loss characteristics for three high frequency materials have been presented. Although, Ferrite (PC40) is lossier than Permalloy80 (0.5 mil), at the frequencies of interest (25 - 50 kHz), the use of the former is justified on the basis of cost, weight and wide range of shapes. The influence of the leakage flux distribution in the window region, on the copper losses has been demonstrated for various conventional winding arrangements. However, it is seen that in conventionally wound transformers, a considerable amount of leakage flux enters the core, resulting in localized core saturation and hot-spots. This becomes a very critical issue especially for high power high frequency transformers. Coaxially wound transformers are seen to be a viable alternative, in that, the leakage flux is contained within the interwinding space, with very little or none of it permeating the core. Such transformers can also realize multiple benefits of a low distributed and controllable leakage inductance, robust construction, low electromechanical forces and low core and copper losses. Test results on two coaxially wound transformers, with different tube geometries, designed for 50 kW, 50 kHz, primary voltage of 200 V and secondary voltage of 1000 V (two windings) have been presented. Finally, the concept of coaxial winding techniques for three phase transformers is also presented.

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PERFORMANCE CHARACTERIZATION OF A HIGH POWER DUAL ACTIVE BRIDGE DC/DC CONVERTER

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Abstract

This paper describes the analysis, control and performance of a high power, high power density dc/dc converter based on the single-phase dual active bridge topology proposed in [1]. The dual active bridge converter was shown to have very attractive features in terms of low device and component stresses, small filter components, low switching losses (by virtue of zero voltage switching), high power density and high efficiency, bidirectional power flow, buck-boost operation and low sensitivity to system parasitics. For high output voltages, in the order of kilovolts, a cascaded output structure is considered. The impact of snubber capacitance and magnetizing inductance on the soft switching region are discussed. Various control strategies are discussed. In particular, computer simulation results of a current mode controller are presented. Since, the leakage inductance of the transformer is the main energy transfer element, special transformer design techniques (reported in [2]) have been utilized to carefully control this parameter. The layout for a completed prototype 50 kW, 50 kHz unit operating with an input voltage of 200 Vdc and an output voltage of 1600 Vdc is presented. Some experimental results are also presented.

Introduction

The field of high power density dc/dc converters has received a lot of attention in recent years. In particular, for low power converters, there has been a proliferation of resonant, quasi-resonant, multi-resonant and resonant transition converters which offer the advantages of soft switching and high switching frequencies [3-6]. By way of contrast, very little has been done in the area of high power dc/dc converters which are subject to similar power density constraints. Schwarz was the first to explicitly recognize the benefits of resonant switching for the realization of dc/dc converters rated in the tens of kilowatts [7]. Although series and parallel resonant converters have since been applied in X-Ray, welding and traction applications, resonant converters in high power applications demand a significant penalty in terms of device and component VA stresses. As a result, hard-switching pulse width modulated dc/dc converters have been the topology of choice in the past.

A more attractive approach for higher power levels is the family of resonant transition or pseudo-resonant converters. These converters have been demonstrated to have very moderate component ratings and low switching loss. The dual active bridge (DAB) converter, proposed in Reference [1], has been shown to be an attractive alternative for high power applications. The converter uses active devices on both the input and output sides to realize a minimal topology which has low device stresses, no extra reactive components, and which uses the transformer leakage inductance as the main energy transfer element. The ripple current levels in the output and input filter capacitors is also seen to be reasonable. The topology also permits high frequency operation as a result of zero voltage switching for all the devices over a reasonable operating range. The DAB converter is also seen to be the dual of a converter proposed by Mohan and Peterson for Superconducting Magnetic Energy Storage Systems (SMES), and has also been referred to as the inductor-converter bridge (ICB) [8,9]. The use of thyristors in the ICB, in particular in a hard switching environment, restricts the maximum frequency attainable. Further, the need for transformer isolation would cause serious problems due to the energy trapped in the leakage inductance. Consequently, the DAB topology is considered to be more attractive, especially where power density is important.

This paper presents the performance characteristics of a high power DAB dc/dc converter for aerospace applications. The converter has been designed with power density as the primary objective. The converter is rated at 50 KW with an input of 200 volts and an output of 1600 volts and is aimed at establishing a modular concept for high voltage output supplies. The unique combination of high frequency, high output voltage and an active output bridge can only be met with a series connected output structure. This paper presents a brief analysis of the topology including parasitic and snubber effects, control techniques for bi-directional power flow using voltage or current mode controllers, and experimental results verifying operation of the converter. Power density figures attained with this converter are also presented.

Analysis

In Reference [1] the analysis of the single phase dual active bridge dc/dc converter, with a single full bridge converter on the output side, was presented. The principle of operation of the dual active bridge dc/dc converter is very simple. Two active bridges are interfaced through a transformer and are phase-shifted from each other to control the amount of power flow, from one dc voltage source to the other. This allows a fixed frequency, square wave mode of operation, and utilization of the leakage inductance of the transformer as the main energy transfer element. The use of a series resonant converter suggests itself, but is not considered attractive because of high VA stresses on all the components.

The high output voltage requirement of 1600 Vdc would seem to make the use of active output bridges difficult, as devices rated in the kilovolt range are limited in terms of switching speed. Also, the high power density needed mandates a high switching frequency. Thus, a series modular approach is necessary for realizing high power at the high output voltages. For the specified output voltage, a cascaded connection of two active half-bridges is used, as shown in Figure 1a. The two secondary side bridges are identically phase-shifted from the input bridge. Figure 1b shows the relevant operating waveforms. The output power, under idealized conditions, is given as,

$$P_O = \frac{2V_i^2}{X_L} d\phi \left(1 - \frac{|\phi|}{\pi}\right) \qquad \ldots(1)$$

where, $X_L = \omega L$, $d = \dfrac{V_o}{2NV_i}$

and, V_i is the input dc voltage, V_o is the output dc voltage of one half-bridge, ω is the switching frequency in radians/sec, L is the primary-referred leakage inductance, N is the transformer turns ratio, and ϕ is the phase-shift between the input and output bridges. Figure 2 shows the family of output power versus phase-shift curves with d as the parameter, for both "motoring" and "regenerating" modes of operation. The "motoring" mode of operation corresponds to positive phase-shifts, that is, the source side bridge leading the load side bridge. In the "regenerative" mode,

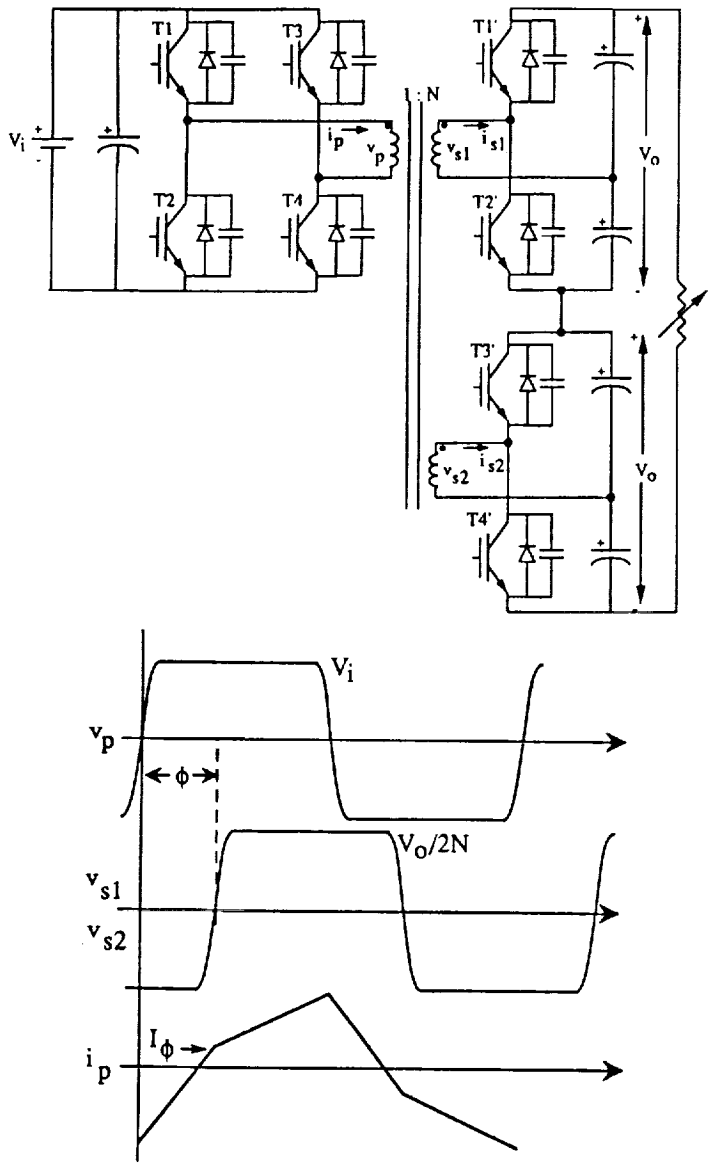


Fig. 1 a) Schematic of DAB DC/DC converter with series connected half bridges on the output.
b) Relevant operating waveforms.

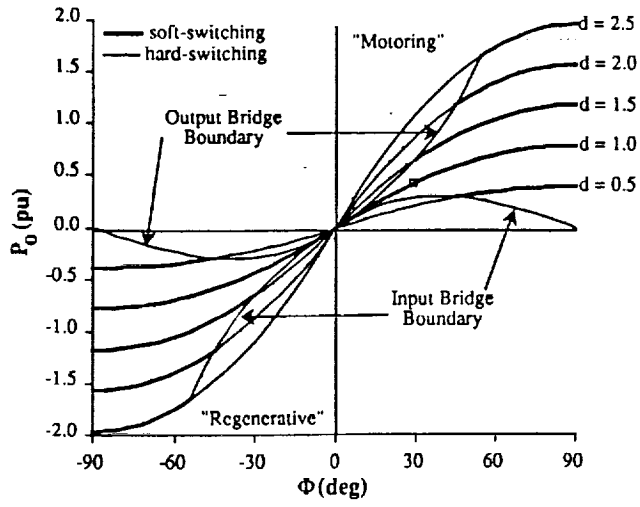


Fig. 2 Output power versus phase-shift, with d as a parameter, showing "motoring" and "regenerating" modes of operation.

the load side bridge leads the source side bridge. The region of soft-switching for all the devices on all the bridges is also identified. Full control range, under soft-switching, is achievable for d = 1, and hence is chosen as a convenient design point. For buck (d < 1) or boost (d > 1) operation the control range is reduced under soft-switching conditions in both the quadrants.

For the power supply designer, a more useful piece of information is the output voltage versus output current characteristic for the converter. This set of information is presented as a nomogram in Figure 3. The bold curves indicate the region of operation of the dual active bridge converter under soft switching conditions of all the devices. Full control under soft switching is achievable at d = 1. Under lightly loaded conditions, as R --> ∞, the soft switching region decreases. The intersection of the constant d-lines and the constant R-lines (load lines) gives a value of the control parameter, ϕ. Similarly, the intersection of the constant ϕ-lines and the constant R-lines indicates an operating point for the converter. Such a nomogram is very useful in ascertaining, rather quickly, if an operating point is within the soft switching region or not.

The above analysis has been carried out under the assumptions that the transformer magnetizing inductance is infinite and the snubber capacitances are negligible. The following sections study the impact of these parameters on the soft switching region of operation for the dual active bridge dc/dc converter.

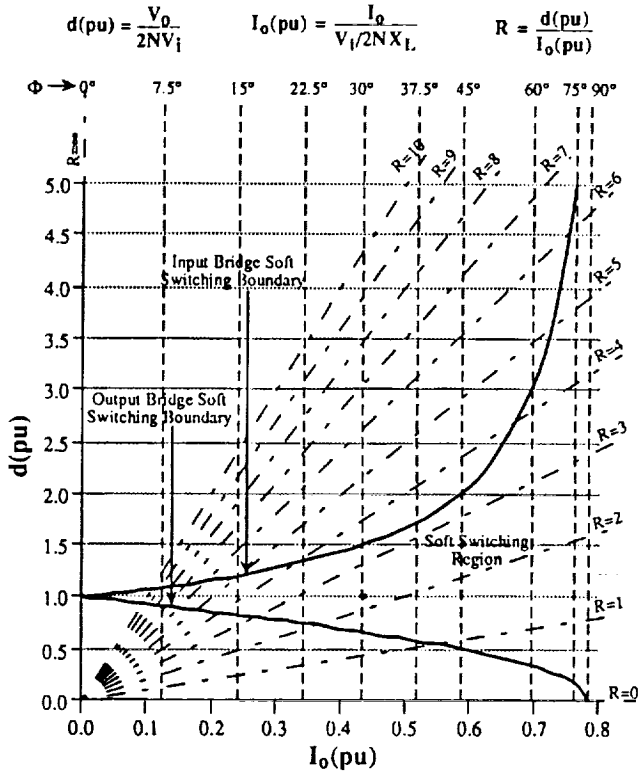


Fig. 3 Nomogram of output voltage versus output currents for DAB converter.

Influence of Transformer Magnetizing Inductance on the Soft Switching Boundaries

This section analyzes the influence of the transformer magnetizing inductance on the soft switching boundaries of the dual active bridge converter. For simplicity only one output half bridge of Figure 1a will be considered. Figure 4 shows the primary referred model for the converter, with the input and output bridges replaced by square wave voltage sources. The T-model has been assumed for the transformer, with half the leakage inductance shown on each side of the finite magnetizing inductance. It is valid to assume that the winding resistances are negligible compared to the leakage reactance at the high frequencies of interest.

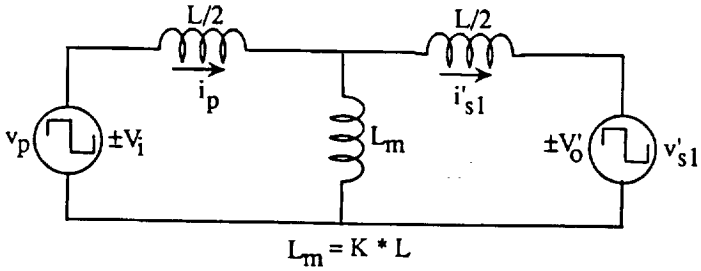


Fig. 4 Primary referred T-model of transformer,considering one secondary winding.

Let the magnetizing inductance, L_m, be K*L, where L is the total leakage inductance and $K \geq 1$. The currents i_p and i_{s1}' can be expressed as,

$$\frac{di_p}{d\theta} = K_1 v_p - K_2 v'_{s1} \qquad ...(2)$$

$$\frac{di'_{s1}}{d\theta} = K_2 v_p - K_1 v'_{s1} \qquad ...(3)$$

where,

$$K_1 = \frac{1 + \frac{1}{2K}}{X_L(1 + \frac{1}{4K})} \qquad ...(4a)$$

and,

$$K_2 = \frac{1}{X_L(1 + \frac{1}{4K})} \qquad ...(4b)$$

and $\theta = \omega t$.

Two modes of operation can be identified for the converter. Solving for the currents and then enforcing the soft switching (zero voltage switching) constraints for the devices on the two bridges, which are,

(i) at turn on of any device, its anti-parallel diode is conducting, and

(ii) at turn off of any device the minimum current through the device is zero,

we get,

For the input bridge:

$$d \leq \frac{K_1}{K_2}\left[\frac{\pi}{\pi - 2\phi}\right] \qquad 0 \leq \phi \leq \frac{\pi}{2} \qquad ...(5a)$$

and,

For the output bridge:

$$d \geq \frac{K_2}{K_1}\left[1 - \frac{2\phi}{\pi}\right] \qquad 0 \leq \phi \leq \frac{\pi}{2} \qquad ...(5b)$$

The normalized average output current, I_o, can be evaluated to be,

$$I_o = K_2 X_L \phi\left[1 - \frac{\phi}{\pi}\right] \qquad ...(6)$$

To illustrate the influence of the magnetizing inductance, the soft-switching region of the converter is depicted on the output voltage versus output current plane for two values of K (Figure 5). $K = 10^5$ represents a large value of the magnetizing inductance. K = 1, although not realistic, represents the other extreme for the magnetizing inductance. It is seen that for low values of the output current, the region of soft-switching widens as K decreases. However, the maximum average output current, governed by the $\phi = \pi/2$ boundary diminishes with decreasing K. The parameter K allows a mechanism for trading off control range over d achievable under soft switching.

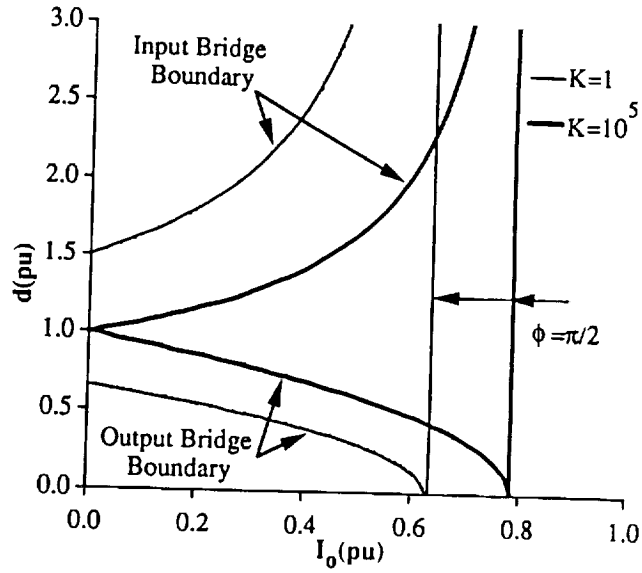


Fig. 5 Effect of magnetizing inductance on the soft-switching region for the DAB converter.

Influence of Snubber Capacitance on the Soft Switching Boundaries

The purpose of this section is to study the influence of snubber capacitance on the minimum current required in the leakage inductance of the transformer during turn-off of any of the devices on either of the input or output bridges. It is shown here that with increasing values of snubber capacitance, the minimum current required for zero voltage switching of any of the devices increases. This would further restrict the region available for soft-switching on the output voltage versus output current plane.

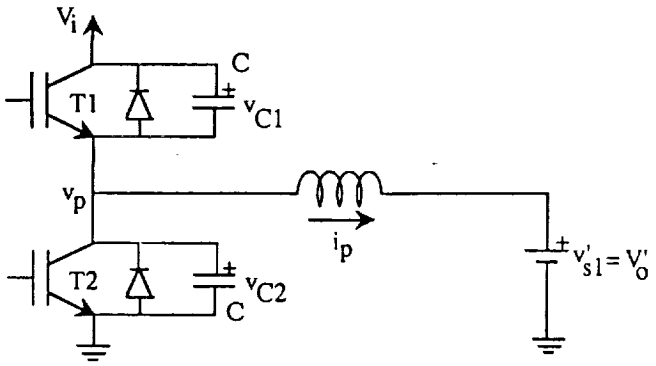
Figure 6a shows one pole of the input bridge. L represents the leakage inductance of the transformer. C is the snubber capacitance across each of the input bridge devices, T1 and T2. The effect of snubber capacitance on the minimum current required through L, for zero-voltage switching on the input devices only, will be considered. Let us assume that at t = 0, the device T1 turns-off, as shown in Figure 6b. All other devices shown in Figure 6a are not conducting at this instant of time. The turn-off time of the device will be considered negligible, and the value of C sufficiently large to ensure very little change in the voltage across T1 during its turn-off interval. Once the device turns off, the inductor current resonates through the snubber capacitances. The current, i_p, flows through L in the direction shown in Figure 6a. The output bridge is replaced by a primary-referred voltage source, V_o', with the proper polarity. We need to find the minimum inductor current required at t = 0, which ensures that the voltage across T1 reaches the clamping value (V_i) when i_p reaches zero. Let $t = t_m$ be the instant of time at which i_p resonates to zero. Hence,

at t = 0,

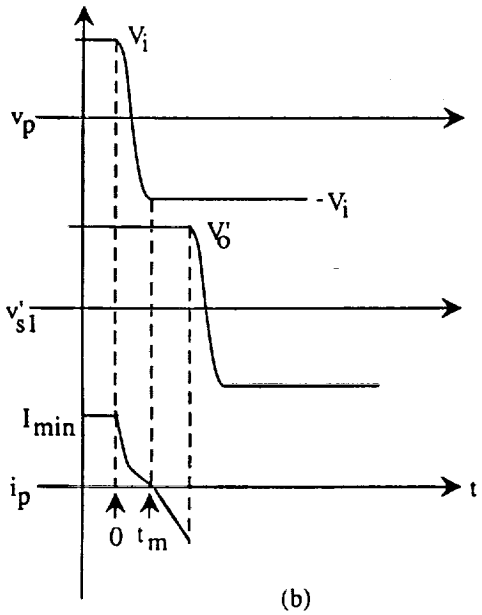
$$i_p = I_{min}, \quad v_{C1} = 0, \quad v_{C2} = V_i$$

and, at $t = t_m$

$$i_p = 0, \quad v_{C1} = V_i, \quad v_{C2} = 0$$



(a)



(b)

Fig. 6 a) A resonant pole of the input bridge.
b) Minimum inductor current required at instant of turn-off of T1, to resonate the pole voltage from $+V_i$ to $-V_i$.

During, the interval $0 \le t \le t_m$,

$$i_p = C\frac{dv_{C1}}{dt} + C\frac{dv_{C2}}{dt} \qquad ...(7)$$

But,

$$\frac{dv_{C1}}{dt} = \frac{dv_{C2}}{dt} = \frac{dv_C}{dt}(say) \qquad ...(8)$$

Hence, from Equations (7) and (8), we get,

$$i_p = 2C\frac{dv_C}{dt} \quad \text{during } 0 \le t \le t_m \qquad ...(9)$$

From, energy balance considerations,

$$E_{(t=0)} = E_{(t=t_m)} + E_{loss} + E_{delivered}$$

Assuming, lossless circuit elements, we get,

$$\frac{1}{2} L I_{min}^2 = E_{delivered} \qquad ...(10)$$

Now,

$$E_{delivered} = \int_0^{t_m} V_o' \, i_p \, dt$$

Substituting for i_p from Equation (9), we get,

$$E_{delivered} = 2CV_o' \int_0^{t_m} v_C$$

Zero voltage switching condition, dictates that the $dv_C = V_i$ during the interval $0 \le t \le t_m$, Hence,

$$E_{delivered} = 2CV_o'V_i \qquad ...(11)$$

Substituting $E_{delivered}$ from Equation (11), into Equation (10), we get,

$$I_{min} = \frac{2}{Z_o}\sqrt{V_i \, V_o'} \quad \text{where, } Z_o = \sqrt{\frac{L}{C}} \qquad ...(12)$$

Normalizing I_{min} with respect to $\frac{V_i}{\omega L}$ and defining $\omega_o = \frac{1}{\sqrt{LC}}$, we get,

$$I_{min(pu)} = \frac{2}{\omega_n}\sqrt{d} \qquad ...(13)$$

$$\text{where, } d = \frac{V_o'}{V_i} \qquad \omega_n = \frac{\omega_o}{\omega}$$

and ω is the switching frequency in rads/sec.

Figure 7 shows a family of curves of $I_{min(pu)}$ versus d with ω_n as the parameter. For a given value of L, ω and d, I_{min} increases, as C increases. Also, for a fixed value of L, ω and C, I_{min} increases as d increases.

It can be seen that as C is increased, switching losses decrease. However, the minimum current requirement imposed by Equation (13) restricts the output voltage-output current region that can be reached under soft switching conditions. Consequently, this becomes an important limit and needs to be explored further in detail. This is done by incorporating the simultaneous influence of the snubber capacitance on the output bridge devices. It should be noted that the decrease in VA-plane due to C is compensated, at least in part, by the impact of the transformer magnetizing inductance.

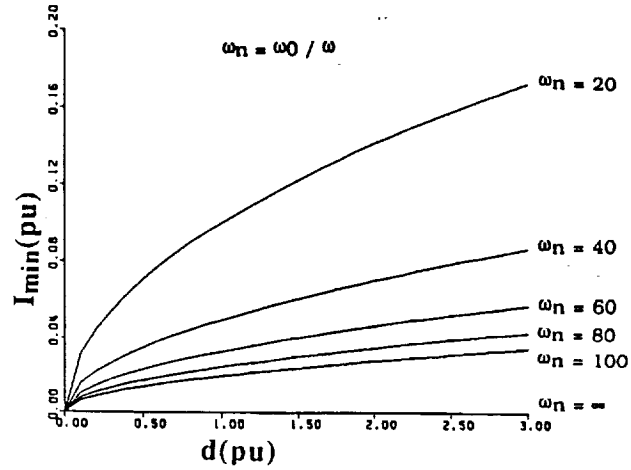


Fig. 7 Minimum required inductor current versus d with ωn as parameter

Control Strategies

Voltage Mode Control

Various control schemes for output voltage control can be implemented. The simplest control scheme is a voltage controller which modifies the phase shift between the primary and secondary bridges dependent on the error in the output voltage. A P-I controller could be used to minimize steady state error. Limits also need to be set to insure device soft switching.

Current Mode Control

A current control strategy is also possible for this type of converter, and is shown in Figure 8. The current command is derived from the voltage error after being processed through a Proportional-plus-Integral compensator. This scheme allows inherent current limiting, and the dynamics of the overall system are reduced to that of a single order system. Figure 9a shows the simulation results of the voltage regulating capability of the controller under startup and step load change conditions. The transformer current waveforms during the step load change are shown in Figure 9b. The results indicate reasonably good dynamic response of the controller.

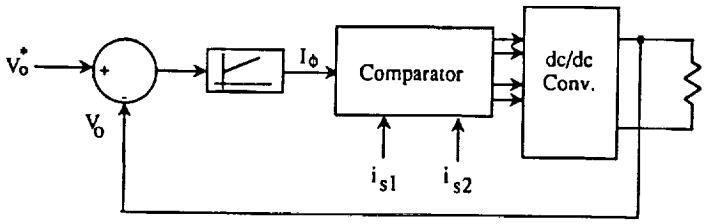


Fig. 8 Block schematic of current mode controller for the DAB converter

Mode-Hopping Control

As seen from Figure 3, under light to no load conditions the region of soft switching is drastically reduced. This implies that in maintaining the output voltage under light loads, the converter may have to be hard switched. A possible solution is found by recognizing the bidirectional power flow capability of the dual active bridge converter. Under light load conditions, a "mode-hopping" strategy can be implemented, wherein the system is cycled sequentially between the "motoring" and "regenerating" modes of operation to maintain the desired average output voltage. This allows the converter to remain in the soft switching region, even while operating at a point which would otherwise be in the hard switching region.

Extending Converter Operating Region

The dual active bridge converter, in essence, has another topological variation. With the output bridge working as a diode bridge, the two poles of the input bridge can be controlled in a phase delay manner to control the amount of power flow. Such a topology was reported in Reference [1], and was referred to as Topology A. This mode of operation allows only unidirectional power flow, and a restricted range of control. Figure 10 shows a superposition of the output voltage versus output current characteristics, under soft switching, of the two topological modes of operation. Topology B mode is the dual active version. It is seen from this figure that a wider range of control is achievable, with soft switching. At high load currents, tight control on the load current can be maintained as the output voltage is reduced, by essentially switching from Topology B mode to Topology A mode as the common soft switching boundary is crossed. A significant implication of this is that the load current could be held constant even under short-circuit faults, with the devices always operating under soft switching conditions.

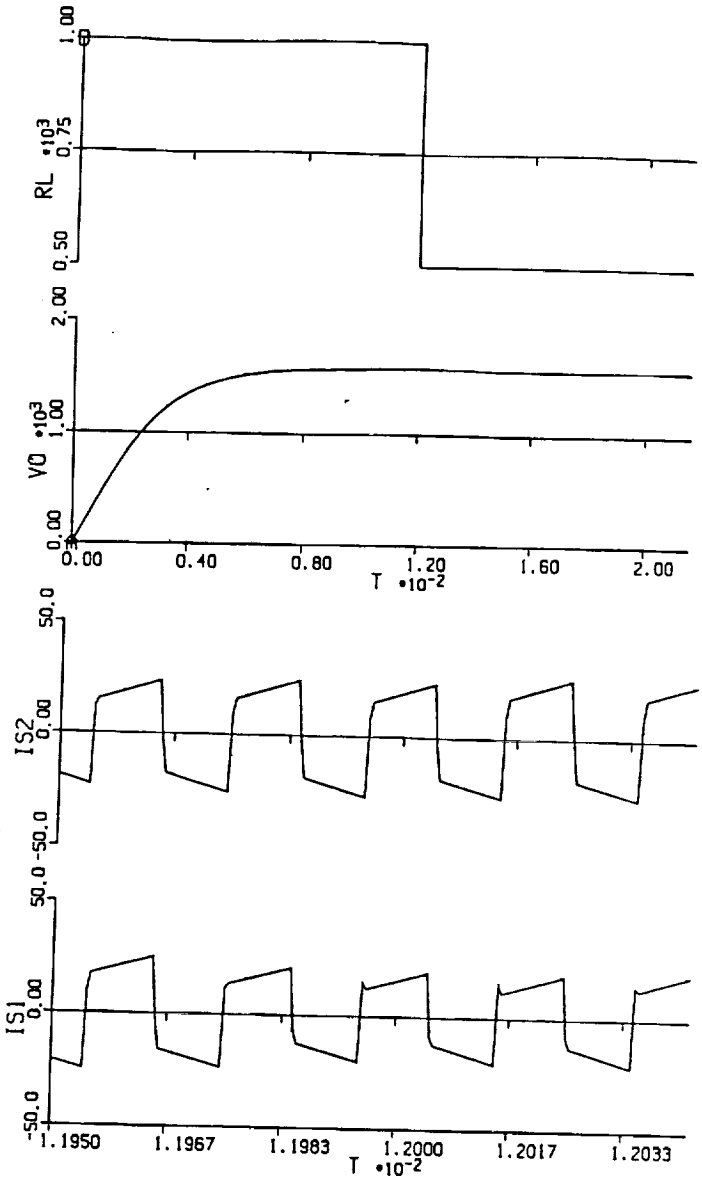


Fig. 9 a) Computer simulation showing regulation of total output voltage at 1600 V during start-up and step load change.
b) Computer simulation of secondary currents during step load change.

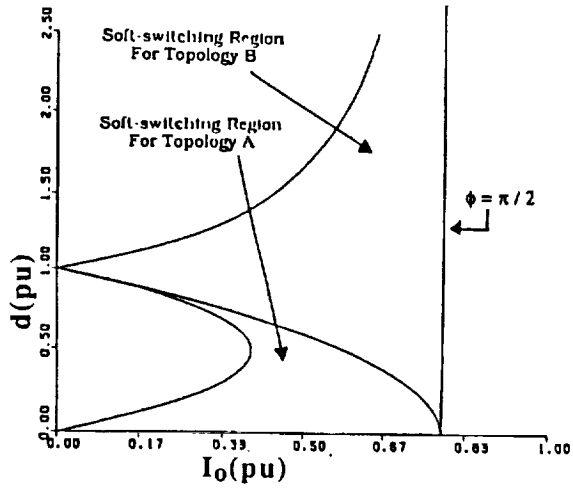


Fig.10 Superposition of the soft switching region for topology A and B (DAB) on the output voltage versus output current plane.

Experimental Results

Converter Description

Figure 11 shows the layout of the 50 kW, 50 kHz Dual Active Bridge converter, which has been fabricated in the laboratory. The schematic of the converter is shown in Figure 1a. To realize the high power densities and minimize the parasitics, multi-layer planar power busses and decoupling techniques have been used. The switching devices used are Insulated Gate Bipolar Transistors (IGBTs). Multi-Layer Ceramic capacitors (MLCs) with high RMS current handling capabilities, very low ESRs (at the operating frequency and higher), and high energy densities have been utilized to realize the input and output filters. The snubber capacitance on the input bridge is 0.1μF per device. Silvered Mica capacitors have been used for this purpose. The snubber capacitance on the output side is in the order of 20 nF per device.

Since the leakage inductance of the transformer is utilized as the main energy transfer element, it must be carefully controlled. Such a design objective is relatively difficult to meet in conventional transformers. A shell-type transformer with coaxial windings, details of which are reported in [2], has been fabricated, to meet the above requirement. Since the majority of the leakage flux is confined to within the interwinding space, the leakage inductance can be reasonably controlled to the desired amount by varying this interwinding space. Moreover, since the leakage flux is not allowed to permeate the core, core losses due to localized saturation are virtually eliminated. The two litz wire wound secondaries, each consisting of 6 turns, are enclosed in a 3 turn primary made of rectangular copper wave guides fabricated into "U" shapes. The core consists of 3 pairs of PC40 Ferrite E-E cores. The power density of the completed transformer is 0.083 kg/kW for a power transfer of 46 kW at 50 kHz. Total transformer losses have been measured as 250 W for the same power transfer giving a projected efficiency of 99.4%. Figure 12 shows oscillograms of the transformer primary current and secondary voltage under short circuit test conditions at 50 KHz. The primary referred magnetizing inductance is 250 μH, while the leakage inductance has been measured at 150 nH.

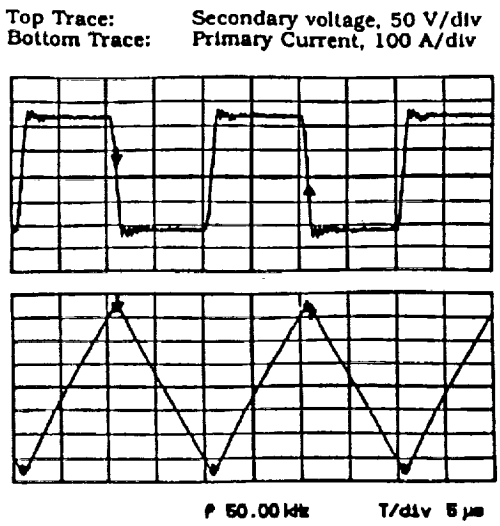


Fig.12 Oscillograms of the rectangular coaxial transformer under short circuit test conditions at 50 KHz.

The overall converter power density is in excess of 7(W/cu.in. and is to a large part governed by the size of the IGBT modules. A weight power density figure has been calculated to be 5000 watts/kg [10] and is also seen to be dominated by device package weight. The entire converter is water-cooled, with the water circulating through the cold plates shown. The hardware for the water cooling system is not shown in the layout.

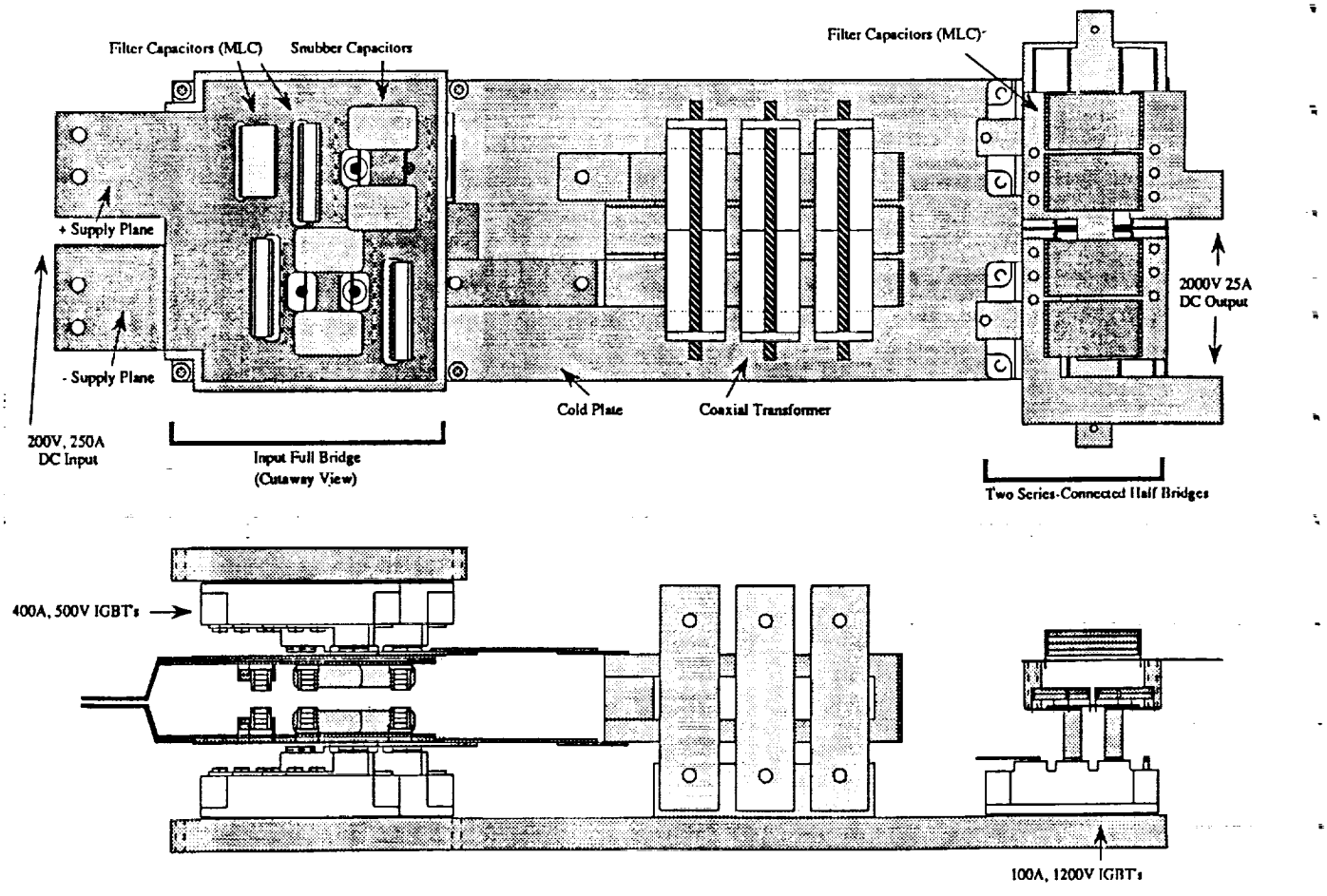


Fig.11 Layout of the 50 KW, 50 KHz DAB DC/DC converter.

Results

Figure 13 shows oscillograms of the DAB converter with only one output bridge connected. The top trace is primary voltage. The oscillations on the primary voltage are due to a substantial amount of stray inductance in the device package. The input voltage was rated voltage of 200 Vdc. At this operating point 6.2 KW of power was transferred to the load, and the efficiency obtained was 91 %.

Figure 14 shows oscillograms of the two secondary windings. The two output half bridges were connected in series to obtain a total output voltage of 1128 Vdc for a power transfer of 3.8 KW at an efficiency of 91 %.

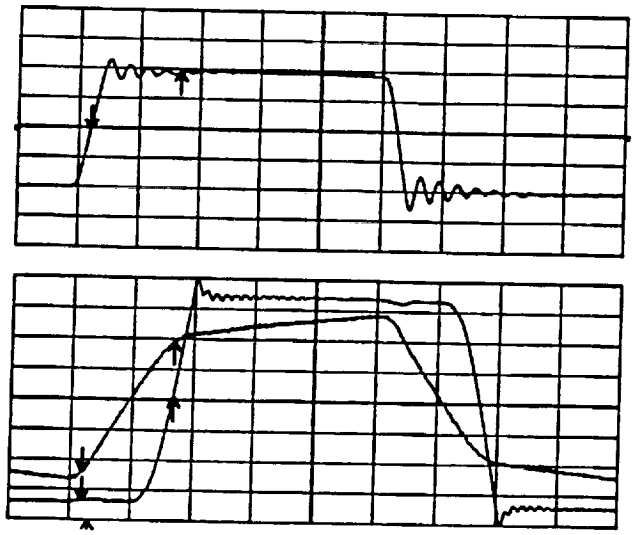


Fig. 13 Oscillograms of the DAB converter with only one output half bridge. Top Trace : Primary voltage, 100 V/div; Bottom Trace : Secondary voltage, 100 V/div; Secondary Current, 10 A/div; Time Scale : 5 μs/div.

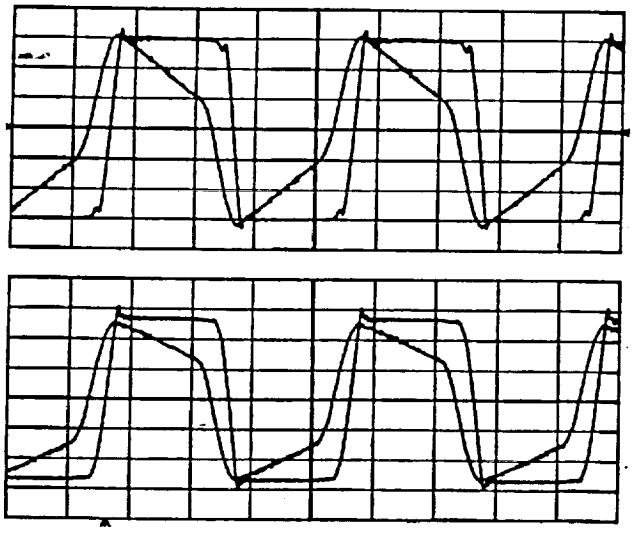


Fig. 14 Oscillograms of the two secondary windings, with series connected output half bridges. Top Traces : Secondary voltage on winding 1, 100 V/div, Secondary current on winding 1, 5 A/div; Bottom Traces : Secondary voltage on winding 2, 100 V/div, Secondary current on winding 2, 5 A/div;

Conclusions

This paper has presented a discussion of the design issues related to a series connected dual active bridge converter. The impact of parasitic elements including the snubber capacitors and the magnetizing inductance was described. Various control strategies possible were discussed. Finally, the fabrication of a DAB converter rated at approximately 50 KW was presented along with power density figures attained. The converter is presently undergoing full testing. As of now, the converter has been operated at up to 8 KW, limited by the present test set-up, with all observable thermal parameters being within specification. The transformer has been tested under rated conditions and the losses have been characterized. No problems were found in terms of voltage sharing in the cascaded converter connection. It is expected that the converter will shortly be tested at its rated power level.

The most significant problem was found to be the device package. Commercially available IGBT modules are not suitable for high-density high-frequency applications because of large size and high internal inductance. Significant gains in performance and power density would be possible with improved device packages. Further, the system losses are seen to be dominated by device conduction losses. The advent of lower forward voltage IGBTs and new MOS Controlled Thyristors would substantially further increase the efficiency of the system. To conclude, the DAB converter has been shown to be a viable topology for high power dc/dc converter applications in which power density constraints are important.

Acknowledgements

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